Zero to Mastery In COMPUTER ARCHITECTURE AND ORGANISATION

Zero to Mastery In COMPUTER ARCHITECTURE AND ORGANISATION

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UNIT-I

Chapter 1

Introduction To Computer

1.0 OBJECTIVES

After going through this chapter you will be able to understand:-

- Concept of Computer, Bytes & Word.
- · Software and its Classification
- Memory features & Classification
- Von Neumann & Flynn Classification of Computer
- Understand the Decimal, Binary, Octal and Hexadecimal Number Systems convert from one Number System into Another
- · Apply Arithmetic Operations to Binary Numbers
- · Understand BCD Codes and Alpha Numeric Codes Learn the Operations of Logic Gates
- · Apply the Basic Laws of Boolean Algebra
- · Apply De Morgan's theorems to Boolean Expressions

1.1 INTRODUCTION

Computer is one of the major components of an Information Technology network and gaining increasing popularity. Today, computer technology has permeated every sphere of existence of modern man. In this chapter, we will introduce to you the computer Concept of computer, Software and its types, Memory, Flynn classification, the binary number system and its relationship to other systems such as decimal, hexadecimal, and octal, Arithmetic operations with binary numbers are also discussed to provide a basis for understanding how computers and many other types of digital systems work. Binary Coded Decimal (BCD), and alpha numeric codes are also introduced. Binary logic gates are explained with the help of logic diagram, block diagram and truth table. Basic laws of Boolean algebra are given. De- Morgan's theorems are also stated and proved, how does it work and what is it?

1.2 WHAT IS COMPUTER?

Computer is defined in the Oxford dictionary as "An automatic electronic apparatus for making calculations or controlling operations that are expressible in numerical or logical terms". A device that accepts data, processes the data according to the Instructions provided by the user, and

finally returns the results to the user and usually consists of input, output, storage, arithmetic, logic, and control units. The computer can store and manipulate large quantities of data at very high speed

The basic function performed by a computer is the execution of a **program.** A program is a sequence of instructions, which operates on data to perform certain tasks.

1.2.1Concept of Digits, Byte & Word

In modern digital computers data is represented in binary form by using two symbols 0 and 1, which are called binary digits or bits. But the data which we deal with consists of numeric data and characters such as decimal digits 0 to 9, alphabets A to Z, arithmetic operators (e.g. +, -, etc.), relations operators (e.g. =, >, etc.), and many other special characters (e.g.;,@, {,],etc.). Thus, collection of eight bits is called a **Byte**. Thus, one byte is used to represent one character internally. Most computers use two bytes or four bytes to represent numbers (positive and negative) internally. Another term, which is commonly used in computer, is a **Word**. A word may be defined as a unit of information, which a computer can process, or transfer at a time. A word, generally, is equal to the number of bits transferred between the central processing unit and the main memory in a **single step**. It may also be defined as the basic unit of storage of integer data in a computer. Normally, a word may be equal to 8, 16, 32 or 64 bits. The terms like 32 bit computer, 64 bit computers etc. basically points out the **word size** of the computer.

1.3 WHAT IS COMPUTER SOFTWARE?

Computer software, or just software, is a collection of computer programs and related data that provide the instructions for telling a computer what to do and how to do it.

Or

Software is a conceptual entity which is a set of computer programs, procedures, and associated documentation concerned with the operation of a data processing system.

Or

Software is a set of programs, procedures, algorithms and its documentation.

Therefore, we can say software refers to one or more computer programs and data held in the storage of the computer for some purpose.

Types of Software: Basically there are THREE categories of software:

- (a) System Software: System software provides the basic functions for computer usage and helps run the computer hardware and system. It includes a combination of the following:
 - Device drivers
 - Operating systems
 - Servers
 - Utilities
 - Window systems

System software is responsible for **managing a variety of independent hardware components**, so that they can work together harmoniously. Its purpose is to unburden the application software programmer from the often complex details of the particular computer being used, including such accessories as communications devices, printers, device readers, displays and keyboards, and also to partition the computer's resources such as memory and processor time in a safe and stable manner.

- (b) **Programming Software:** Programming software usually provides tools to assist a programmer in writing computer programs, and software using different programming languages in a more convenient way. The tools include:
 - Compilers
 - Debuggers
 - Interpreters
 - Linkers
 - Text editors

An Integrated development environment (IDE) is a single application that attempts to manage all these functions.

- (c) Application Software: Application software is developed to aid in any task that benefits from computation. It is a broad category, and encompasses software of many kinds, including the internet browser, this category includes:
 - Business software
 - Computer-aided design
 - Databases
 - Decision making software
 - Image editing
 - Industrial automation
 - Mathematical software
 - Medical software
 - Molecular modeling software
 - Simulation software
 - Spreadsheets
 - Video games
 - · Word processing

1.3.1 Opearting Systems

An operating system (OS) is software, consisting of programs and data, which runs on computers, manages computer hardware resources, and provides common services for execution of various application software.

Or

An operating system is similar to a government... Like a government, the operating system performs no useful function by itself. (A. Silberschatz, P. Galvin)

Or

The most fundamental of all systems programs is the operating system, which controls all the computer's resources and provides the basis upon which the application programs can be written. (A.S. Tanenbaum)

Examples: Solaris, HP-UX, AIX, Linux, BSD, MAC OS X, Windows (Microsoft), MAC OS (Apple), OS/2 (IBM), MVS (IBM), OS/390 (IBM), BS 2000 (Siemens) VxWorks, Embedded Linux, Embedded BSD, TinyOS

1.3.2 Hardware vs. System vs. Application

- From the operating system perspective, the hardware is mainly characterized by the machine instruction set.
- The operating system is part of the system software which includes system libraries and tools.
- Applications are build on top of the system software.



Fig:1.1 View of H/W, S/S & A/S

1.3.3 Services provided by OS for Application Programs

- Loading of programs
- Execution of programs (management of processes)
- · High-level input/output operations
- Logical file systems (open (), write (),)
- · Control of peripheral devices
- · Interprocess communication primitives
- Network interfaces
- · Checkpoint and restart primitives

1.3.4 Various classification of OS

Real-time Operating System

A real-time operating system is a multitasking operating system that aims at executing real-time applications. Real-time operating systems often use specialized scheduling algorithms so that they can

achieve a deterministic nature of behavior. The main object of real-time operating systems is their quick and predictable response to events. They either have an **event-driven** or a **time-sharing** design. An event-driven system switches between tasks based on their priorities while time-sharing operating systems switch tasks based on clock interrupts.

Multi-user vs. Single-user

A multi-user operating system allows multiple users to access a computer system concurrently. **Time-sharing system** can be classified as multi-user systems as they enable a multiple user access to a computer through the sharing of time.

Single-user operating systems, as opposed to a multi-user operating system, are usable by a single user at a time. Being able to have multiple accounts on a **Windows operating system does not make it a multi-user system.** Rather, only the network administrator is the real user. But for a **Unix-like operating system**, it is possible for two users to login at a time and this capability of the OS makes it a multi-user operating system.

Multi-tasking vs. Single-tasking

When a single program is allowed to run at a time, the system is grouped under a single-tasking system, while in case the operating system allows the execution of multiple tasks at one time, it is classified as a **multi-tasking operating system**. Multi-tasking can be of two types namely, **pre-emptive or co-operative**.

In pre-emptive multitasking, the operating system slices the CPU time and dedicates one slot to each of the programs. Unix-like operating systems such as Solaris and Linux support pre-emptive multitasking. **Cooperative multitasking** is achieved by relying on each process to give time to the other processes in a defined manner. MS Windows prior to Windows 95 used to support cooperative multitasking.

Distributed

A distributed operating system manages a group of independent computers and makes them appear to be a single computer. The development of networked computers that could be linked and communicate with each other, gave rise to distributed computing. Distributed computations are carried out on more than one machine. When computers in a group work in cooperation, they make a distributed system.

Embedded

Embedded operating systems are designed to be used in embedded computer systems. They are designed to operate on small machines like PDAs with less autonomy. They are able to operate with a limited number of resources. They are very compact and extremely efficient by design. Windows CE and Minix 3 are some examples of embedded operating systems.

1.4. MEMORY UNITS

1.4.1 Introduction

The computer system essentially comprises three important parts - input device, central processing unit (CPU) and the output device. The CPU itself is made of three components namely, the arithmetic logic unit (ALU), memory unit, and the control unit.

In addition to these, auxiliary storage/secondary storage devices are used to store data and instructions on a long-term basis.



Central Processing Unit

Fig. 1.2: CPU and Other Devices

All storage devices are characterized with the following features:

- Speed
- Volatility
- · Access method
- · Portability
- · Cost and capacity
- Latency
- Band-Width

1.4.2 Basic Units of Measurement

All information in the computer is handled using electrical components like the integrated circuits, semiconductors, all of which can recognize only two states-presence or absence of an electrical signal. Two symbols used to represent these two states are 0 and 1, and are known as **BITS** (an abbreviation for BInary DigiTS). 0 represents the absence of a signal, 1 represents the presence of a signal. A **BIT** is, therefore, the smallest unit of data in a computer and can either store a 0 or 1.

Since a single bit can store only one of the two values, there can possibly be only four unique combinations: $00\ 01\ 10\ 11$

Bits are, therefore, combined together into larger units in order to hold greater range of values.

BYTES are typically a sequence of eight bits put together to create a single computer alphabetical or numerical character. More often referred to in larger multiples, bytes may appear as Kilobytes (1,024 bytes), Megabytes (1,048,576 bytes), Giga Bytes (1,073,741,824), Tera Bytes (approx. 1,099,511,000,000 bytes), or PetaBytes (approx. 1,125,899,900,000,000 bytes).

Bytes are used to quantify the amount of data digitally stored (on disks, tapes) or transmitted (over the internet), and are also used to measure the **memory and document size.**

1.4.3 Memory Hierarchy

Memory hierarchy starts with a small, expensive, and relatively fast unit, called the **cache**, followed by a larger, less expensive, and relatively slow **main memory unit**. Cache and main memory are built using solid-state semiconductor material (typically CMOS transistors). It is customary to call the fast memory level the primary memory. The solid-state memory is followed by larger, less expensive, and far slower magnetic memories that consist typically of the (hard) disk and the tape. It is customary to call the disk the **secondary memory**, while the tape is conventionally called the **tertiary memory**. The objective behind designing a memory hierarchy is to have a memory system that performs as if it consists entirely of the fastest unit and whose cost is dominated by the cost of the slowest unit.



Fig. 1.3: Depicts a typical memory hierarchy

Table 1.0 provides typical values of the memory hierarchy parameters

	Access type	Capacity	Latency	Bandwidth	Cost/MB
CPU registers	Random	64-1024 bytes	1-10 ns	System clock rate	High
Cache memory	Random	8-512 KB	15-20 ns	10-20 MB/s	\$500
Main memory	Random	16-512 MB	30-50 ns	1-2 MB/s	\$20-50
Disk memory	Direct	1-20 GB	10-30 ms	1-2 MB/s	\$0.25
Tape memory	Sequential	1-20 TB	30-10,000 ms	1-2 MB/s	\$0.025

1.4.4 Cache Memory

Cache memory owes its introduction to Wilkes back in 1965. At that time, Wilkes distinguished between two types of main memory: The **conventional** and the **slave memory**. In Wilkes terminology, a slave memory is a second level of unconventional high-speed memory, which nowadays corresponds to what is called cache memory (the term cache means a safe place for hiding or storing things).

The idea behind using a cache as the first level of the memory hierarchy is to keep the information expected to be used more frequently by the CPU in the cache memory.

1.4.5 RAM, ROM, PROM, EPROM

Computer's Primary memory can be classified into two types - RAM and ROM.

RAM or Random Access Memory: It is characterize by following features:

- It is the central storage unit in a computer system.
- It is the place in a computer where the operating system, application programs and the data in current use are kept temporarily so that they can be accessed by the computer's processor
- The more RAM a computer has, the more data a computer can manipulate.
- Random access memory, also called the **Read/Write memory**, is the temporary memory of a computer.
- It is said to be 'volatile' since its contents are accessible only as long as the computer is on. The contents of RAM are cleare once the computer is turned off.

ROM or Read Only Memory: It is characterize by following features:

- It is a special type of memory which can only be read and contents of which are not lost even when the computer is switched off. It typically contains manufacturer's instructions.
- ROM also stores an initial program called the 'bootstrap loader' whose function is to start the computer software operating, once the power is turned on.
- Read-only memories can be: manufacturer-programmed or user-programmed.
- · Manufacturer-programmed ROMs have data burnt into the circuitry.
- User programmed ROMs can have the user load and then store read-only programs.
- PROM or Programmable ROM is the name given to such ROMs.

Information once stored on the ROM or PROM chip cannot be altered.

However, another type of memory called EPROM (Erasable PROM) allows a user to erase the information stored on the chip and reprogram it with new information. EEPROM (Electrically EPROM) and UVEPROM (Ultra Violet EPROM) are two types of EPROM's.

1.4.6 Primary Vs. Secondary Memory

RAM is volatile memory having a limited storage capacity. Secondary/auxiliary storage is storage other than the RAM. These include devices that are peripheral and are connected and controlled by the computer to enable permanent storage of programs and data.

Magnetic medium was found to be fairly inexpensive and long lasting medium and, therefore, became the preferred choice for auxiliary storage. Floppy disks and hard disks fall under this category. The newer forms of storage devices are optical storage devices like CDs, DVDs, Pen drive, Zip drive etc.

1.4.7 Auxiliary Storage Devices-Magnetic Tape, Floppy Disk, Hard Disk, PAN-Drive

The Magnetic Storage Exploits duality of magnetism and electricity. It converts electrical signals into magnetic charges, captures magnetic charge on a storage medium and then later regenerates electrical current from stored magnetic charge. Polarity of magnetic charge represents bit values zero and one.

Magnetic Disk

The Magnetic Disk is Flat, circular platter with metallic coating that is rotated beneath read/write heads. It is a Random access device; read/write head can be moved to any location on the platter.

Floppy Disk

These are small removable disks that are plastic coated with magnetic recording material. Floppy disks are typically 3.5" in size (diameter) and can hold 1.44 MB of data. This portable storage device is a rewritable media and can be reused a number of times.

Hard Disk

Another form of auxiliary storage is a hard disk. A hard disk consists of one or more rigid metal plates coated with a metal oxide material that allows data to be magnetically recorded on the surface of the platters. The hard disk platters spin at a high rate of speed, typically 5400 to 7200 revolutions per minute (RPM).

Storage capacities of hard disks for personal computers range from 10 GB to 120 GB (one billion bytes are called a gigabyte).



PAN-Drive: A USB flash drive consists of a flash memory data storage device integrated with a USB (Universal Serial Bus) interface. USB flash drives are typically removable and rewritable, and physically much smaller than a floppy disk. Most weigh less than 30 g. Storage capacities in 2012 can be as large as 256 GB with steady improvements in size and price per capacity expected.

Fig. 1.6: Pan-Drive





Fig 1.4:Floppy Disk

1.4.8 Optical Disks: CD-R Drive, CD-RW disks, DVD, Blue ray Discs

Optical Mass Storage Devices Store bit values as variations in light reflection. They have higher area density & longer data life than magnetic storage. They are also Standardized and relatively inexpensive. Uses: read-only storage with low performance requirements, applications with high capacity requirements & where portability in a standardized format is needed.

Example of the Optical Drives CD's (Compact Disk)

Storage: 700 MB storage

Types:

- CD-ROM (read only)
- CD-R: (record) to a CD
- CD-RW: can write and erase CD to reuse it (re-writable)
- DVD(Digital Video Disk)

CD: Compact Disk (CD): It is portable disk having data storage capacity between 650-700 MB. It can hold large amount of information such as music, full-motion videos, and text etc. It contains digital information that can be read, but cannot be rewritten. Separate drives exist for reading and writing CDs. Since it is a very reliable storage media, it is very often used as a medium for distributing large amount of information to large number of users. In fact today most of the software is distributed through CDs.

DVD Digital Versatile Disk (DVD): It is similar to a CD but has larger storage capacity and enormous clarity. Depending upon the disk type it can store several Gigabytes of data(as opposed to around 650MB of a CD). DVDs are primarily used to store music or movies and can be played back on your television or the computer too. They are not rewritable media. It's also termed DVD (Digital Video Disk)

DVD-ROM

- Over 4 GB storage (varies with format)
- DVD- ROM (read only)
- Many recordable formats (e.g., DVD-R, DVD-RW; ..)
- Are more highly compact than a CD.
- Special laser is needed to read them

Blu-ray Technology

The name is derived from the blue-violet laser used to read and write data. It was developed by the Blu-ray Disc Association with more than 180 members. Some companies with the technology are Dell, Sony, LG.The Data capacity is very largebecause Blu-ray uses a blue laser(405 nanometers) instead of a red laser(650nanometers) this allows the data tracks on the disc to be very compact. This allows for more than twice as small pits as on a DVD. Because of the greatly compact data Bluray can hold almost 5 times more data than a single layer DVD. Close to 25 GB!.Just like a DVD Blu-ray can also be recorded in Dual-Layer format. This allows the disk to hold up to 50 GB.

The Variations in the formats are as follows:

- BD-ROM (read-only) for pre-recorded content
- BD-R (recordable) for PC data storage

- BD-RW (rewritable) for PC data storage
- BD-RE (rewritable) for HDTV recording

1.5 VON NEUMANN ARCHITECTURE

Most of today's computer designs are based on concepts developed by John von Neumann referred to as the VON NEUMANN ARCHITECTURE. Von Neumann proposed that there should be a unit performing arithmetic and logical operation on the data. This unit is termed as **Arithmetic Logic (ALU)**. One of the ways to provide instruction to such computer will be by connecting various logic components in such a fashion, that they produce the desired output for a given set of inputs. The process of connecting various logic components in specific configuration to achieve desired results is called **Programming**. This programming since is achieved by providing instruction within hardware by various connections is termed as Hardwired and when the programming is performed on software components is known as soft-wired.

The following figure shows the basic structure of von Neumann machine. A von Neumann machine has only a **single path** between the main memory and control unit (CU). This feature/ constraint is referred to as **von Neumann bottleneck**.

Several other architectures have been suggested for modern computers.

- A von Neumann architecture for computer consist of following attributes
- · Treats Program and Data equally
- · One port to Memory
- · Simplified Hardware
- "von Neumann Bottleneck" (rate at which data and program can get into the CPU is limited by the bandwidth of the interconnect)



Fig. 1.7:von Neumann Machine

1.6 FLYNN'S CLASSIFICATION OF COMPUTER

According to Flynn's classification of computer can be categorized into following categories

1.6.1 Single Instruction Single Data (SISD)

The classical von Neumann machine can be regarded as a Single-Instruction-Single -Data machine in that at a time only a single instruction is being executed, and only a single piece of data is being operated upon. This is arises of the problem, since we often want to execute the same instruction on many different pieces of data, and the von Neumann machine requires us to fetch the same instruction many times, once for each piece of data. In fact the situation is much worse since a von Neumann machine will usually require us to create a loop, and so we will need to execute many instructions for each piece of data.

This can slow the machine down many times over what the arithmetic unit is capable of performing operations.

1.6.2 Multiple Instruction Single Data (MISD)

The Multiple Instruction Single Data (MISD) architecture is the most uncommon, In this architecture, the same data stream flows through a linear array of processors, executing different instructions on the single Data stream. This kind of architecture is also known as a **systolic array** for pipelined execution of specific algorithms.

1.6.3 Multiple Instruction Multiple Data (MIMD)

The most general form of von Neumann architecture is the Multiple-Instruction-Multiple-Data machine. A MIMD machine is consist of a number of separate processors connected together through some interconnection network. The actual format of interconnection between the processors can take many forms, depending on the type of problem, which the machine is designed to solve. This is the most common architecture chosen for multiple processor machines because modern processors have the control logic for parallel systems built in. Therefore, this is attractive since software, replacement parts and additions to the system are easily accessible.

1.7 NUMBER SYSTEMS

A number system relates quantities and symbols. The base or radix of a number system represents the number of digits or basic symbols in that particular number system. In decimal system the base is 10, because of use the numbers 0,1,2,3,4,5,6,7,8 and 9.

1.7.1 Binary Number System

A binary number system is a code that uses only two basic symbols. The digits can be any two distinct characters, but it should be 0 or 1. The binary equivalent for some decimal numbers are given below

Decimal	0	1	2	3	4	5	6	7	8	9	10	11
Binary	0	01	10	11	100	101	110	111	1000	1001	1010	1011

Each digit in a binary number has a value or weight. The LSB has a value of 1. The second from the right has a value of 2, the next 4, etc.,

16	8	4	2	1
24	2 ³	2 ²	21	20

Binary to decimal conversion:

 $\begin{array}{rl} (1001)2 &= X_{10} \\ 1001 = 1 \times 2^3 &+ 0 \times 2^2 &+ 0 \ge 2^1 &+ 1 \times 2^0 \\ &= 8 + 0 + 0 + 1 &(1001)_2 = (9)_{10} \end{array}$

Fractions:

For fractions the weights of the digit positions are written from right of the binary point and weights are given as follows.

2-1 2-2	2-3	2-4	2-5
---------	-----	-----	-----

E.g.:

$$(0.0110)_2 = X_{10} = 0 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3} + 0 \times 2^{-4} = 0 \times 0.5 + 1 \times 0.25 + 1 \times 0.125 + 0 \times 0.0625 = (0.375)_{10}$$

E.g.:

$$(1011.101)_2 = X_{10}$$

= 1 × 2³ + 0 × 2² + 1 × 2¹ + 1 × 2⁰ + 1 × 2⁻¹ + 0 × 2⁻² + 1 × 2⁻³
= 8 + 0 + 2 + 1 + 0.5 + 0 + 0.125 = (11.625)_{10}

Decimal to binary conversion: (Double Dabble method)

In this method the decimal number is divided by 2 progressively and the remainder is written after each division. Then the remainders are taken in the reverse order to form the binary number.

E.g.:

$$(12)_{10} = X_{2}$$

$$2 12 - 0 - 0$$

$$2 3 - 0 - 1$$

$$(12)_{10} = (1100)_{2}$$

E.g.:

$$(21)_2 = X_2$$

$$(21)_2 = (10101)_2$$

Fractions:

The fraction is multiplied by 2 and the carry in the integer position is written after each multiplication. Then they are written in the forward order to get the corresponding binary equivalent. *E.g.*:

 $\begin{array}{l} (0.4375)_{10} = X_2 \\ 2 \times 0.4375 = 0.8750 \rightarrow 0 \\ 2 \times 0.8750 = 1.750 \rightarrow 1 \\ 2 \times 0.750 = 1.5 \rightarrow 1 \\ 2 \times 0.5 = 1.0 \rightarrow 1 \\ (0.4375)_{10} = (0.0111)_2 \end{array}$

1.7.2 Octal Number System

Octal number system has a base of 8 i.e., it has eight basic symbols. First eight decimal digits 0, 1,2,3,4,5,6,7 are used in this system.

Octal to decimal conversion:

In the octal number system each digit corresponds to the powers of 8. The weight of digital position in octal number is as follows

84	8 ³	82	8 ¹	80	8-1	8-2	8_3
----	----------------	----	----------------	----	-----	-----	-----

To convert from octal to decimal multiply each octal digit by its weight and add the resulting products.

E.g.:

$$(48)_8 = X_{10}
4_8 = 4 \times 8^1 + 7 \times 8^0
= 32 + 7
= 39
(48)_8 = (39)_{10}$$

E.g.:

$$(22.34)_8 = X_{10}$$

$$22.34 = 2 \times 8^1 + 2 \times 8^0 + 3 \times 8^{-1} + 4 \times 8^{-2}$$

$$= 16 + 2 + 3 \times 1/8 + 4 \times 1/64$$

$$= (18.4375)$$

$$(22.34)_8 = (18.4375)_{10}$$

Decimal to octal conversion

Here the number is divided by 8 progressively and each time the remainder is written and finally the remainders are written in the reverse order to form the octal number. If the number has a fraction part, that part is multiplied by 8 and carry in the integer part is taken. Finally the carries are taken in the forward order.

E.g.:

$$(19.11)_{10} = X_8$$

$$8 \boxed{19}{2-3}$$

$$0.11 \times 8 = 0.88 \rightarrow 0$$

$$0.88 \times 8 = 7.04 \rightarrow 7$$

$$0.04 \times 8 = 0.32 \rightarrow 0$$

$$0.32 \times 8 = 2.56 \rightarrow 2$$

$$0.56 \times 8 = 4.48 \rightarrow 4 (19.11)10 = (23.07024)_8$$

Octal to binary conversion

Since the base of octal number is 8, i.e., the third power of 2, each octal number is converted into its equivalent binary digit of length three.

E.g.:

$(57.127)_8 = X_2$								
5	7		1	2	7			
101	111		001	010	111			
$(57.127)_8 = (101111001010111)_2$								

Binary to octal

The given binary number is grouped into a group of 3 bits, starting at the octal point and each group is converted into its octal equivalent.

E.g.:

$$(1101101.11101)_2 = X_8$$

001	101	101		111	010
1	5	5	•	7	2

(1101101.11101)₂

 $=(155.72)_{8}$

1.7.3 Hexadecimal Number System

The hexadecimal number system has a base of 16. It has 16 symbols from 0 through 9 and A through F.

Decimal	Hexadecimal	Binary
0	0	0000
1	1	0001
2	2	0010
3	3	0011
4	_4	0100

5	5	0101
6	6	0110
7	7	0111
8	8	1000
9	9	1001
10	А	1010
11	В	1011
12	C	1100
13	D	1101
14	Е	1110
15	F	1111

Binary to hexadecimal:

The binary number is grouped into bits of 4 from the binary point then the corresponding hexadecimal equivalent is written.

E.g.:

 $(100101110 . 11011)_2 = X_{16}$

Hexadecimal to binary

Since the base of hexadecimal number is 16, i.e., the fourth power of 2, each hexadecimal number is converted into its equivalent binary digit of length four.

E.g.:

 $(5D. 2A)_{16} = X_2$ 5 D . 2 A 0101 1101 . 0010 1010 $(5D. 2A)_{16} = (01011101.00101010)_2$

Decimal to hexadecimal

The decimal number is divided by 16 and carries are taken after each division and then written in the reverse order. The fractional part is multiplied by 16 and carry is taken in the forward order.

E.g.:

 $(2479.859)_{10} = X_{16}$

$$\begin{array}{c} 16 \ \underline{2479} \\ 16 \ \underline{154} \\ 9 \\ -10(A) \end{array}$$

 $16 \times 0.859 = 13.744 \Longrightarrow 13$ (D) $16 \times 0.744 = 11.904 \Longrightarrow 11$ (B) $16 \times 0.904 = 14.464 \Longrightarrow 14$ (E) $16 \times 0.464 = 7.424 \Longrightarrow 7$ $16 \times 0.424 = 6.784 \Longrightarrow 6$ $(2479.859)_{10} = (9AF.DBE76)_{16}$

Hexadecimal to decimal

Each digit of the hexadecimal number is multiplied by its weight and then added.

E.g.:

$$(81.21)_{16} = X_{10}$$

= 8 x 16¹ + 1 x 16⁰ + 2 x 16⁻¹ + 1 x 16⁻²
= 8 x 16 + 1 x 1 + 2/16 + 1/162
= (129.1289)_{10}
(81.21) 16 = (129.1289)_{10}

1.7.4 Binary Arithmetic

Binary Addition

To perform the binary addition we have to follow the binary table given below.

0 + 0 = 0

0 + 1 = 1

$$1 + 0 = 1$$

 $1 + 1 = 0 \rightarrow \text{plus a carry-over of } 1$

Carry-overs are performed in the same manner as in decimal arithmetic. Since 1 is the largest digit in the binary system, any sum greater than 1 requires that a digit be considered over.

111	1010	11.01
<u>110</u>	<u>1101</u>	<u>101.11</u>
1001	<u>10111</u>	1001.00

E.g.

Binary Subtraction

To perform the binary subtraction the following binary subtraction table should be followed.

 $\begin{array}{l} 0 - 0 = 0 \\ 1 - 0 = 1 \\ 1 - 1 = 0 \\ 0 - 1 = 1 \end{array}$ with a borrow of 1 is equivalent to 10 - 1 = 1 **E.g.:** 111 <u>010</u> <u>101</u>

E.g.:

110.01 <u>100.10</u> 001.11

1's complement:

To obtain 1's complement of a binary number each bit of the number is subtracted from 1.

E.g.:

Binary number	1's Complement
0101	1010
1001	0110
1101	0010
0001	1110

Thus 1's complement of a binary number is the number that results when we change each 0 to a 1 and each 1 to a 0.

1's complement subtraction

Instead of subtracting the second number from the first, the 1's complement of the second number is added to the first number. The last carry which is said to be a END AROUND CARRY, is added to get the final result.

E.g.:

$$\begin{array}{cccc}
7 & \longrightarrow 111 & + \\
\underline{-3} & 100 & + \\
\hline
4 & 1011 & + \\
& & \underline{-1} \\
\hline
100 & (\text{ result})
\end{array}$$

If there is no carry in the 1's complement subtraction, it indicates that the result is a negative and number will be in its 1's complement form. So complement it to get the final result.

E.g.:

 $\begin{array}{cccc}
8 & \longrightarrow & 1000 & + \\
-10 & 1'^{s} \text{ complement} & \\
4 & & \\
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The following points should be noted down when we do 1's complement subtraction.

- 1. Write the first number (minuend) as such.
- 2. Write the 1's complement of second number(subtrahend)
- 3. Add the two numbers.
- 4. The carry that arises from the addition is said to be "end around carry".
- 5. End-around carry should be added with the sum to get the result.

6. If there is no end around carry find out the 1's complement of the sum and put a negative sign before the result as the result is negative.

2's Complement:

2's complement results when we add '1' to 1's complement of the given number i.e.,

2's complement =1's complement + 1

Binary Number	1's complement	2's complement
1010	010	0110
0101	1010	1011
1001	0110	0111
0001	1110	1111

2's Complement Subtraction

Steps:

- 1. Write the first number as such
- 2. Write down the 2's complement of the second number.
- 3. Add the two numbers.
- 4. If there is a carry, discard it and the remaining part (sum) will be the result (positive).
- 5. If there is no carry, find out the 2's complement of the sum and put negative sign before the result as the result is negative.

10 - 1010 -8 1000 2's co

$$\frac{1000}{10010}$$

Therefore Result is $(0010)_2$

E.g.:2

- $5 0101 \longrightarrow 0101 +$
- 12 1100 2's complement 0100
- 4 1001 2's complement 1001 Therefore Result is $(-0111)_2$

 \longrightarrow 1010 +

Binary Multiplication

The table for binary multiplication is given below

 $0 \times 0 = 0$ $0 \times 1 = 0$ $1 \times 0 = 0$ $1 \times 1 = 1$ *E.g.:*

$\begin{array}{r} 1011 \times 110 \\ 1011 \times \\ \underline{110} \\ 0000 \\ 1011 \end{array}$

<u>1011</u> 1000010

E.g.:

```
\begin{array}{r} 101.01 \times 11.01 \\ 101.01 \times \\ \underline{11.01} \\ 101 \ 01 \\ 00000 \\ 10101 \\ \underline{10101} \\ 10001.0001 \end{array}
```

Binary division

The table for binary division is as follows.

 $0 \div 1 = 0$

 $1 \div 1 = 1$

As there fore result is $(-0111)_2$ n the decimal system division by zero is meaning less.

```
E.g.: 1) 1100÷11
```

$$\begin{array}{c}
11 \\
11 \\
1100 \\
11A \\
0 \\
11A \\
0 \\
2) 1001 \div 10
\end{array}$$



1.7.5 BCD Addition

Binary Coded Decimal(BCD) is a way to express each of the decimal digits with a binary code. There are only ten code groups in the BCD system. The 8421 code is a type of BCD code. In BCD each decimal digit, 0 through 9 is represented by a binary code of four bits. The designation of 8421 indicates the binary weights of the four bits $(2^3, 2^2, 2^1, 2^0)$. The largest 4-bit code is 1001. The numbers 1010, 1011, 1100, 1101, 1110, and 1111 are called forbidden numbers. The following table represents the decimal and 8421 equivalent numbers.

Decimal digit	0	1	2	3	4	5	6	7	8	9
BCD	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001

8421 ADDITION

In 8421 addition, if there is a carry or if it results in a forbidden group, then 0110 (decimal equivalent 6) should be added in order to bring the result to the 8421 mode again.

E.g.:

 $8+1000 + 7 0111 \\ 15 1111 \\ + 0110 \\ 00010101 \\ 15 1000 \\ 1000$

```
E.g.:
```

 $18 {+} 0001 1000 {+} $

- 2 0000 0010
- 20 0001 1010
- + 0000 0110

0010 0000

1.7.6 Alphanumeric Code

Computers, printers and the other devices must process both alphabetic and numeric information. Serial coding systems have been developed to represent alphanumeric information as a series of 1's and 0's. The characters to be coded are alphabets(26), numerals (10) and special characters such as +,-,/, *, \$ etc,

1

In order to code a character, string of binary digits is used. In order to ensure uniformity in coding, two standard codes have been used.

- 1. ASCII: American Standard Code for Information Interchange.
- 2. EBCDIC: Extended Binary Coded Decimal Interchange Code. It is an 8 bit code.

ASCII is 7-bit code of the form X6, X5, X4, X3, X2, X1, X0 and is used to code two types of information. One type is the printable character such as alphabets, digits and special characters. The other type is known as control characters which represent the coded information to control the operation of the digital computer and are not printed.

Check Your Progress 1

1.	2×1	$0^{1} + 8 \times 10^{0}$ is equal	to					
	(a)	10	(b)	280	(c)	2.8	(d)	28
2.	The	binary number 110	1 is e	equal to the decimal nun	nber			
	(a)	13	(b)	49	(c)	11	(d)	3
3.	The	decimal 17 is equal	l to t	he binary number				
	(a)	10010	(b)	11000	(c)	10001	(d)	01001
4.	The	sum of 11010 + 01	111 ¢	equals				
	(a)	101001	(b)	0101010	(c)	110101	(d)	101000
5.	The	difference of 110 -	010	equals				
	(a)	001	(b)	010	(c)	101	(d)	100
6.	The	1's complement of	1011	1001 is				
	(a)	01000111	(b)	01000110	(c)	11000110	(d)	10101010
7.	The	2's complement of	1100	01000 is				
	(a)	00110111	(b)	00110001	(c)	01001000	(d)	00111000
8.	The	binary number 101	1001	11001010100001 can b	e wri	tten in octal as		
	(a)	54712308	(b)	54712418	(c)	26345218	(d)	231625018
9.	The	binary number 100	0110	1010001101111 can be	writt	en in hexadecim	nal as	1
	(a)	AD46716	(b)	8C46F16	(c)	8D46F16	(d)	AE46F16
10.	The	BCD number for d	ecim	al 473 is				
	(a)	111011010	(b)	1110111110101001	(c)	010001110011	(d)	01001111001

1.8 REVIEW QUESTIONS

- Q.1 Describe BITS, BYTES, WORD.
 Q.2 Discuss Von Neumann classification of Computer.
 Q.3 What are the parameters that characteristics SIMD computers?
 Q.4 How System Software differ to Application Software?
 Q.5 Briefy explain the characteristics of memory devices in a memory hierarchy.
- **Q.6** Write the features of RAM, ROM.
- **Q.7** What is the purpose of cache?
Q.8 How is it used?

Q.9 How the memories represented on memory hierarchy?

Q.10 What are SISD, SIMD, MISD, MIMD, and differentiate each?

1.9 SUMMARY

Byte consist of 8 bits

Word may be defined as a unit of information, which a computer can process, or transfer at a time.

Software's may be Application, System & Programmed

Memory may be Primary(RAM,ROM) & Auxiliary (TAPE,DISK)

Flynn Classification computer may be SISD, SIMD, MISD, MIMD

Von Neumann computer have three main components and have single path between main memory & Components

Binary Number is a weighted number in which the weight of each whole number digit is a positive power of 2 and the weight of each fractional digit is a negative power of 2.

1's Complement of a binary number is derived by changing 1s to 0s and 0s to 1s

2's Complement of a binary number can be derived by adding 1 to the 1's complement.

Octal Number system consists of eight digits, 0 through 7.

Hexadecimal number system consists of 16 digits and characters, 0 through 9 followed by A through F.

ASCII is a 7-bit alphanumeric code that is widely used in computer systems for input/output of information.

1.10 CHECK YOUR PROGRESS 1

1. (d)	2. (a)	3. (c)	4. (a)
5. (d)	6. (b)	7. (d)	8. (b)
9. (c)	10. (c)		

Chapter 2

Logic Gates & Boolean Algebra

2.0 OBJECTIVES

After going through this chapter you will be able to understand:-

- · Concept of Discrete System
- Logic gates: AND, OR, NOT, NOR, NAND, XOR
- Concept of Boolean Algebra
- · Concept of De-Morgan Theory

2.1 INTRODUCTION

A system is simply any entity which generates **output from input**. A system may have any given number of input and output ports. The name **"port"** is derived from the analogy with shipping. We may make use of the mathematical concept of a function to describe how each possible input value causes a particular output value. The statement of system function then serves to define a particular system.

By Time-Discrete System (Figure 2.1) is meant one whose output changes only at regular, discrete intervals of time. The intervals may be thought of as ending with each tick of a system clock. Regardless of any change to the input, no change of output will take place until the clock ticks. Any system which does not wait for the tick of a clock is called a **continuous system**.



Fig. 2.1: Time discrete System

Digital systems use an internal representation of abstract quantities by first assigning it a distinct integer value and then representing each digit separately. In contrast, **Analog systems** represent a varying abstract quantity (e.g. temperature) by varying a physical quantity which serves as its analog. If such a system is implemented using electrical technology the physical analog may be a current or voltage Binary representation has a distinct advantage which greatly simplifies implementation. The machine need only physically represent two digit values, 0 and 1.

Digital systems are thus not able to internally represent any value an abstract quantity may take.

Before encoding it must be quantized, Quantization means the selection of the nearest allowed value. The computer is a special type of **Time-discrete Digital System** and is programmable.

Before discussing the Logic Gates we need to understand following common terms used in description: **Bit:** A binary digit; can have a value of 0 or 1

Logic Diagram: A diagram showing an interconnection of logic symbols.

Truth Table: The truth table gives the input-output relation of a logic gate or logic circuit in tabular form. It specifies the output bit(s) for each possible input bit combination. A circuit with n binary inputs has 2^n different input combinations. A binary value of 0 is sometimes referred to as L (low) or F (false). A binary value of 1 is sometimes referred to as H (high) or T (true). A truth table of n binary inputs has 2^n minterms and an output is specified for each.

Min Terms: are easily deducible from a truth table, by writing down the pattern which produces each 1 of function value and expressed as **Sum of Product**.

Max Terms: are also easily deducible from a truth table, by writing down the pattern which produces each 0 of function value and expressed as **Product of Sum**.

2.1 LOGIC GATES

Logic gates are devices which implement systems with binary input and output values. The presence or absence of a potential, at either input or output, is used to infer the truth or otherwise of a proposition.

OR

A logic gate is an idealized or physical device implementing a Boolean function, that is, it performs a logical operation on one or more logic inputs and produces a single logic output.

OR

A logic gate is simply an electronic circuit which operates a one or more signals to produce an output signal. The output is high only for certain combination of input signals. Gates can be classified into following three categories:

(a) Basic or Fundamentals Gates : AND, OR, NOT

(b) Universal Gates: means that they can be used to make all the others Example NOR, NAND Gates

(c) Derived Gates: X-OR,X-NOR

2.1.1 Basic Or Fundamentals Gates

AND-Gate

An AND gate (Figure 2.2) has a high output only when all inputs are high. The output is low when any one input is low. The is AND operation is also expressed by A^B. Therefore we can say if neither or only one input to the AND gate is HIGH, a LOW output results. In another sense, the function of AND effectively finds the minimum between two binary digits, just as the OR function finds the maximum.



Fig. 2.2: AND gate

Boolean expression for AND gate operation is Y=A, B

Α	В	Y=A.I
0	0	0
0	1	0
1	0	0
1	1	1

Truth Table 2.0: AND gate

OR-Gate

An OR gate (Figure 2.2) produces a high output when any or the entire inputs are high. The output is low only when all the inputs are low. In another sense, the function of OR effectively finds the maximum between two binary digits, just as the complementary AND function finds the minimum The OR operation is also expressed by AVB.



Fig. 2.3: OR gate

The Boolean expression for an OR gate is Y=A+B

Α	В	$\mathbf{Y} = \mathbf{A} + \mathbf{B}$
0	0	0
0	1	1
1	0	1
1	1	1

Truth Table:2.1: OR Gate

NOT gate:

A NOT gate (Figure 2.3) is also called an inverter. The circuit has one input and one output. The output is the complement of the input. If the input signal is high, the output is low and vice versa.



Fig. 2.4: NOT gate

The Boolean expression for NOT gate is

 $Y = \overline{A}$

Α	$Y = \overline{A}$
0	1
1	0

Truth Table:2.2 Not Gate

If two NOT gates are cascaded then the output will be same as the input and the circuit is called **Buffer Circuit**.

2.1.2 UNIVERSAL GATE

NAND- Gate

A NAND (Figure 2.4) gate has two or more input signals but only one output signal. All input signals must be high to get a low output. When one AND gate is combined with a NOT gate, a NAND gate is obtained.



Fig. 2.5: NAND gate

Α	B	$Y = A \cdot B$
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table: 2.3: NAND Gate

NOR- Gate:

NOR gate (Fig. 2.5) has two or more input signals and one output signal. It consists of one OR gate followed by an inverter. A NOR gate produces a high output only when **all the inputs are low**.



Truth Table:2.4 NOR Gate

NAND or NOR to implement a combinational logic system usually turns out to be more efficient in the sense of minimizing production cost, which is of course the most important sense of all.

2.1.3 Derived Gates

XOR gate

XOR (Figure 2.6) gate is an abbreviation of exclusive OR gate. It has two inputs and one output. For a two input XOR gate, the output is high when the inputs are different and the output is low when the inputs are same. In general, the output of an XOR gate is high when the number of its **high inputs** is odd. The Boolean expression of the XOR gate is



Α	В	$\mathbf{Y} = \mathbf{A} \oplus \mathbf{B}$
0	0	0
0	1	1
1	0	1
1	1	0

Truth Table:2.5:XOR Gate

From the truth table of XOR (Table2.5) we note that the operator value is 1 (true) when:

 \overline{A} .B=1

 $A.\overline{B}=1$

These two are called minterms. We know that any Boolean function may be written as either

• Standard sum of products (minterms)

• Standard product of sums (maxterms)

Minterms are easily deducible from a truth table, simply by writing down the pattern which produces each 1 of function value. In X-OR the value of the function is 1 if the first minterm is 1 OR the second OR the third and so on.

Uses of XOR gate: The exclusive-or operator is so useful because...

(i) It inverts (complements) a bit and It is equivalent to binary (modulo 2) addition

(ii) Binary to Gray Converter



Fig. 2.8: Binary to Gray Converter

The Figure 2.7 shows the way to convert binary number to gray number using XOR gates. Since mod-2 addition is involved in the conversion, XOR gate is used for this purpose.

(iii) Gray to Binary Converter: XOR gate is also used to convert gray code to a binary number. The circuit diagram for this operation is shown in the Figure 2.8.



Fig. 2.9: Gray to Binary Converter

(iv) Parity Checker: Parity checker can be designed using XOR gates as given in the Figure 2.9. Here the parity of the word ABCD is checked. The circuit adds the bits of ABCD. A final sum of 0 implies even parity and a sum of 1 means odd parity.



Fig. 2.10: Parity checker

2.1.4 Positive And Negative Logic

The binary signal at the inputs and outputs of any gate has one of the two values, except during transition. One signal value represents logic-1 and the other logic-0. Since two signal values are assigned to two logic values, there exists two different assignments of signal level to logic value, as shown in Figure. 2.10 The higher signal level is designated by H and the lower signal level is designated by L. Choosing the high-level H to represent logic-1 defines a positive logic system. Choosing the low-level L to represent logic-1 defines a negative logic system.



Fig. 2.11: Signal assignment & Logic Polarity

2.2 BOOLEAN ALGEBRA

The basic rules for simplifying and combining logic gates are called Boolean algebra in honour of George Boole (1815 - 1864) who was a self-educated English mathematician who developed many of the key ideas.

Boolean variables are variables with range $\{1,0\}$. Boolean expressions are equivalent to prepositional formula. They are formed by combining operators and variables, exactly as for ordinary algebra, and evaluate to $\{1,0\}$ as do Boolean variables which may be regarded as primitive expressions. Boolean functions, like Boolean variables, evaluate to the range $\{1,0\}$ only. They may be specified by...

- Boolean expression
- Truth table

The **Truth Table** is a unique specification, i.e. there is only one per function. There are, however, often many expressions for each function. For this reason it is best to initially specify a requirement as a truth table and then proceed to a Boolean expression.

Boolean functions are important to computer architecture because they offer a means of specifying the behaviour of systems in a manner which allows a modular approach to design. Algebraic laws may be employed to transform expressions.

The following set of example will allow you to understand the basic rules:

Example: 1

Consider the AND gate where one of the inputs is 1. By using the truth table, investigate the possible outputs and hence simplify the expression $A \cdot 1$.

Solution From the truth table for AND, we see that if A is 1 then $1 \cdot 1 = 1$, while if A is 0 then $0 \cdot 1 = 0$. This can be summarised in the rule that $A \cdot 1 = A$, i.e.,



Example: 2

Consider the AND gate where one of the inputs is 0. By using the truth table, investigate the possible outputs and hence simplify the expression $A \cdot 0$.

Solution From the truth table for AND, we see that if A is 1 then $1 \cdot 0 = 0$, while if A is 0 then $0 \cdot 0 = 0$. This can be summarised in the rule that $A \cdot 0 = 0$



Example: 3

Obtain the rules for simplifying the logical expressions

- (a) A + 0 which corresponds to the logic gate
- (b) A+1 which corresponds to the logic gate

Solution: 3 (a)

From the truth table for OR, we see that if A is 1 then 1 + 0 = 1, while if A is 0 then 0 + 0 = 0. This can be summarised in the rule that A + 0 = A



3(b) From the truth table for OR we see that if A is 1 then 1 + 1 = 1, while if A is 0 then 0 + 1 = 1. This can be summarised in the rule that A + 1 = 1



Example: 4

Obtain the rules for simplifying the logical expressions:

(a) A + A which corresponds to the logic gate

(b) $A \cdot A$ which corresponds to the logic gate

Solution 4 (a)

From the truth table for OR, we see that if A is 1 then A+A = 1+1 = 1, while if A is 0 then A+A = 0+0 = 0. This can be summarised in the rule that A + A = A



4(b) From the truth table for AND, we see that if A is 1 then $A \cdot A = 1 \cdot 1 = 1$, while if A is 0 then $A \cdot A = 0 \cdot 0 = 0$. This can be summarised in the rule that $A \cdot A = A$



Example: 5

Obtain the rules for simplifying the logical expressions:

(a) A + A' which corresponds to the logic gate x

(b) $A \cdot A'$ which corresponds to the logic gate

Solution 5 (a)

From the truth table for OR, we see that if A is 1 then A + A' = 1 + 0 = 1, while if A is 0 then A + A' = 0 + 1 = 1. This can be summarised in the rule that A + A' = 1



5 (b) From the truth table for AND, we see that if A is 1 then $A \cdot A' = 1 \cdot 0 = 0$, while if A is 0 then $A \cdot A' = 0 \cdot 1 = 0$. This can be summarised in the rule that $A \cdot A' = 0$



Fig. 2.18 (b)

Example: 6

Simplify the logical expression (A')' represented by the following circuit diagram.



Fig. 2.19

Solution From the truth table for NOT we see that if A is 1 then (A')' = (1')' = (0)' = 1, while if A is 0 then (A')' = (0')' = (1)' = 0. This can be summarised in the rule that (A')' = A



The Boolean identities are given as: Commutative law: A + B = B + A B + A = A + BAssociative law: A + (B + C) = (A + B) + C A. (B.C) = (A.B).CDistributive law A. (B + C) = A.B + A.COther laws of Boolean algebra:

1.A + 0 = A2. A + 1 = 13.A + A = A4. A + \overline{A} = 1 5. A .0 = 06. A.1 = A7. A.A = A8. A. $\overline{A} = 0$ = 9. A = A10.A + A.B = A11. A.(A + B) = A12. (A+B).(A+C) = A + B.C13. $A + \overline{A} \cdot B = A + B$ 14. A. $(\overline{A} + B) = A.B$ 15. $(A + B) \cdot (\overline{A} + C) = A \cdot C + \overline{A} \cdot B$ 16. $(A + C) \cdot (\overline{A} + B) = A \cdot B + \overline{A} \cdot C$

2.2.1 De Morgan's Theorems

I Theorem statement:

The complement of a sum is equal to the product of the complements.

 $\overline{A+B} = \overline{A} \cdot \overline{B}$

II Theorem Statement:

The complement of a product is equal to the sum of the complements. Case 3: A = 1, B = 0

L.H.S
$$\Rightarrow \overline{A+B} = \overline{1+0} = \overline{1}+0$$

R.H.S $\Rightarrow \overline{A}.\overline{B} = \overline{1}.\overline{0} = 0.1 = 0$
Case 4:
A = 1, B = 1
L.H.S = $\overline{A+B} = \overline{1+1} = \overline{1} = 0$
R.H.S = $\overline{A}.\overline{B} = \overline{1}.\overline{1} = 0.0 = 0$

A	В	$\overline{\overline{A}} + B$	Ā.B
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

Truth table 2.6

A	В	Ā.B	$\overline{A} + \overline{B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

Truth table 2.7

CHECK YOUR PROGRESS 2

1. An inverter performs an operation	n knowr	n as		
(a) Complementation	(b)	assertion	(c)	Inversion
(d) both answers (a) & (b)				
2. The output of gate is LOW when	at least	one of its inputs	is HIGH.	It is true for
(a) AND	(b)	NAND	(c)	OR
(d) NOR				
3. The output of gate is HIGH when	at least	t one of its inputs	is LOW.	It is true for
(a) AND	(b)	OR	(c)	NAND
(d) NOR				
4. The output of a gate is HIGH if an	nd only	if all its inputs are	e HIGH.	It is true for
(a) XOR	(b)	AND	(c)	OR
(d) NAND				
5. The output of a gate is LOW if an	d only i	f all its inputs are	HIGH. I	t is true for

(a) AND	(b)	XNOR	(c)	NOR
(d) NAND				
6. Which of the following gates canno	t be	used as an inverter?		
(a) NAND	(b)	AND	(c)	NOR
(d) None of the above				
7. The complement of a variable is alw	/ays			
(a) 0	(b)	1	(c)	equal to the variable
(d) the inverse of the variable				
8. Which one of the following is not a	valid	rule of Boolean algeb	ora? (a	a) $A + 1 = 1$
(b) $A = \overline{A}$ (c) $A.A = A$ (d) $A + 0 = A$	A			

9. Which of the following rules states that if one input of an AND gate is always 1, the output is equal to the other input ?

(a)
$$A + 1 = 1$$
 (b) $A + A = A$ (c) $A \cdot A = A$
(d) $A \cdot 1 = A$

2.3 GLOSSARY

Alphanumeric : Consisting of numerals, letters, and other characters.

ASCII: American Standard Code for Information Interchange.

BCD: Binary Coded Decimal; a digit code in which each of the decimal digits, 0 through 9, is represented by a group of four bits.

Binary : Describes a number system that has a base of two and utilizes 1 and 0 as its digits.

Boolean algebra : The mathematics of logic circuits.

Gate: A logic circuit that performs a specified logic operation, such as AND, OR or NOT.

Hexadecimal : Describes a number system with a base of 16

Octal: Describes a number system with a base of 8.

Parity : Parity is based on the number of 1's in a binary word. If the number of 1's in a word is odd, then it is a odd parity word and if the number of 1's is even, then it is an even parity word.

Truth table : A table showing the inputs and corresponding output levels of a logic circuit.

Universal gate : Either a NAND gate or a NOR gate.

2.4 ANSWERS TO CHECK YOUR PROGRESS QUESTIONS

Check Your Progress 2

1.(d) 2.(d) 3.(c) 4.(b) 5.(d) 6.(b) 7.(d) 8.(b) 9.(d)

Chapter 3

Combinational & Sequential Circuits

3.0 OBJECTIVES

At the end of this unit you will be able to describe:

- What are Combinational & Sequential Circuits and their differences?
- What are latches flip-flops and gates?
- Combinational and sequential circuits and their applications thereof.
- Some of the useful circuits of a computer system such as Multiplexers, De-Multiplexer, Decoders, En-coder, Adder, Shift Register etc.
- How a very basic mathematical operation; the addition is performed by a computer.

3.1 COMBINATIONAL LOGIC

Combinational logic consists of **logic gates** (sometimes also referred to as **combinatorial logic**) and is a type of **digital logic** which is implemented by boolean circuits, where the output is a pure function of the present input only.

Or

Implementing a **truth function** by use of **combining logical operators** is known as **combinational logic.**

A combinational circuit performs a specific information-processing operation assigned logically by a set of Boolean functions. Combinatorial Circuits are circuits which can be considered to have the following generic structure



Fig. 3.1: Logic Diagram of combinational Circuit

3.2 SEQUENTIAL LOGIC OR CIRCUIT

Sequential circuits contain logic gates as well as memory cells. Their outputs depend on the present inputs and also on the states of memory elements. Since the outputs of sequential circuits

depend not only on the present inputs but also on past inputs, the circuit behavior must be specified by a time sequence of inputs and memory states. The general structure of Sequential circuit is given as:

Combinational Logic+ Memory Elements



Fig. 3.2: Logic Diagram of Sequential Circuit

Points to Remember

*Unlike combinational logic, sequential circuits have **state**, which means basically, sequential circuits have **memory**.

*The main difference between sequential circuits and combinational circuits is that sequential circuits compute their output based on **input and state**, and that the state is updated based on a clock. Combinational logic circuits implement Boolean functions, so they are functions only of their **inputs**, and are not based on clocks.

*In Practical computer circuits normally contain a **mixture of combinational and sequential logic.** For example, the part of an arithmetic logic unit, or ALU, that does mathematical calculations is constructed using combinational logic. Other circuits used in computers, such as half adders, full adders, half subtractors, full subtractors, multiplexers, demultiplexers, encoders and decoders are also made by using combinational logic.

Différences between combinational & Sequential Logic Circuits				
Combinational Circuit	Sequential Circuit			
1. Outputs depend only on its current inputs.	Outputs depend not only on the current			
	inputs but also on the past sequences of inputs.			
2. A combinational circuit may contain an arbitrary number of logic gates and inverters but no feedback loops.	Sequential logic circuits contain combinational logic in addition to memory elements formed with feedback loops.			
3. A feedback loop is a connection from the output of one gate to propagate back into the input of that same gate.	The behavior of sequential circuits is formally described with state transition tables and diagrams.			
4. The function of a combinational circuit represented by a logic diagram is formally described using logic expressions and truth tables.				

Differences between Combinational & Sequential Logic Circuits

3.3 TYPES OF COMBINATIONAL CIRCUIT

3.3.1 Multiplexer or Data Selector

A multiplexer is a combinational logic circuit, which has **many inputs and only one Output**. (Multiplexer means **"Many to one"**).

OR

In electronics, a **multiplexer or Data selector** is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has n select lines, which are used to select which input line to send to the output.

• Multiplexing: combining many signals into a single transmission circuit or channel

• Multiplexer: An electronic device that accomplishes multiplexing

Figure 3.3 shows a four data input multiplexer. D3, D2, D1 and D0 are data inputs. A and B are control inputs. Y is the output of the multiplexer. (Note that the multiplexer can be obtained by modifying a decoder circuit).

When control input AB=00, Gate=0 is enabled and hence Y=D0. Similarly if AB=10,

Gate 2 is enabled and hence Y=D2 and so on. The truth table and schematic diagram of multiplexer is shown in below





А	В	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

Table 3.1: Truth table for multiplexer (MUX) with four inputs

Applications of Multiplexer

• Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth.

- The multiplexer is also used to switch between channels. It is simply a multi-way switch. An example of a MUX is the channel selector on a television. The source of information for the channel to the system which builds images on the screen is switched between the many available TV broadcast channels.
- Another common use of a MUX is to share a single available channel between multiple sources. For example, there might be only a single telephone cable between two countries. Multiple telephone connections are possible over the single cable if a MUX is connected at the source and its inverse, a DEMUX, at the sink. The sources are rapidly switched in and out such that packets of each conversation are transmitted in sequence. The DEMUX must know this sequence in order to route each packet to the correct receiver. This is known as **time-multiplexing**. The users are unaware that only one physical channel exists. They are said to be exploiting virtual channels.
- MUXs are used in computers for selecting one of a number of binary signals or for sharing limited numbers of physical channels.

Points to Remember

- 1. Defined as a circuit which connects one of input data lines to one output line. In (Means a "Multiplexer" converts multiple input to a single output.)
- 2. The data source selected for connection is determined by a set of n input select lines.
- 3. Architecture consists of a decoder plus an ORing element.
- 4. Data lines D_i are ANDed with decoder minterms to provide selection of data sources.
- 5. Demonstration of multiplexing action as provided by a mechanical switch.
- 6. May also be employed as a SOP Boolean function generator of the input select lines (the data inputs specify the truth table values.)

3.3.2 DEMULTIPLEXER

A demultiplexer performs a function opposite to that of a multiplexer. It has **one data input and several output lines.** Based on the value of the control input, one of the output lines will become active and will output the data input across it. Figure 3.4 shows a 1 to 4 demultiplexer. D is the data input Y3, Y2, Y1 and Y0. ie. Y0=D. Similarly when the control input AB=10, Y2=D.

OR

A DEMUX performs the inverse function of the MUX. A single input value is routed to an output channel selected by the two select control inputs. Figure 3.4 shows the combinational logic required. Its truth table is shown in Table 3.2



Truth Table3.2: 2 By 4 De-multiplexer

A DEMUX may be used to route data to the currently addressed system simply by connecting

Points to Remember

- 1. Defined as a circuit which connects one input data line to one of 2ⁿ output lines
- 2. The output line selected for connection is determined by a set of **n** output select lines.
- 3. Demonstration of demultiplexing action as provided by a mechanical switch.
- 4. A DeMUX circuit can be realized from a decoder circuit by utilizing the decoder enable input line E as the DeMUX data input line.

3.3.3 Decoder

A decoder has several output lines and control input lines. Based on the value of the control input (or select input), one of the output lines will become active.

If there are **four control input lines**, then the decoder can have up to a maximum of sixteen (2 power 4) output lines When the control input AB=00, the AND gate G0 is enabled and its output Y0 is high. Suppose AB=10, then G2 is enabled and hence Y2 will be high.

OR

In digital electronics, a decoder can take the form of a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. e.g. n-to- 2^n , binary-coded decimal decoders. Enable inputs must be on for the decoder to function, otherwise its outputs assume a single "disabled" output code word. The Decoding is necessary in applications such as data multiplexing, 7 segment display and memory address decoding,

A 2-bit decoder has an input consisting of two signals, one for each bit of a binary word, and four separate outputs, one for each input value. Figure 3.5 shows a schematic diagram and the truth table of a 2-bit decoder and fig 3.6 show 3-8 line Decoder.



Fig. 3.5: 2-to-4-Line Decoder with Enable Input



Fig. 3.6: 3 by 8 line De-coder

Applications of De-Coder

- It is widely used as address decoder in a computer system. (The outputs of a decoder can become the select inputs to the memory locations. In such case, the control inputs become the address of the memory location).
- Decoder circuit is used in every important CLC except the encoder.
- The most important use of decoders is in bus communication,

Point to Remember

- 1. Defined as a circuit which translates an n-bit input code word into a larger m bit output word
- 2. Architecture consists of an array of m ANDing elements (active-high outputs use AND gates; active-low outputs use NAND gates)
- 3. For simple decoders, the outputs are **minterms** of the input select line variables.
- 4. The enable signal E must be in the active state to enable the decoder.

5. Simple decoders may also be employed as a **SOP Boolean generator** of the **n select lines.** Sum desired minterms by attaching an **ORing element** to the corresponding decoder outputs (each output line contributes one minterm.)

3.3.4 EN-CODER

An encoder is a digital circuit that generates **the binary code corresponding to the input number**. An octal-to-Binary encoder takes an octal input (in some symbolic form) and generates its binary equivalent as output. Similarly, a **Decimal-to-Binary encoder takes a decimal input and generates an equivalent binary output.** Figure 3.7 shows an Octal-to-Binary encoder using OR gates. (A Decimalto-Binary encoder has ten input lines and uses four OR gates at the output).



Fig. 3.7: Show Octal to binary Encoder

	inputs					0	outputs			
7	6	5	4	3	2	1	0	A	B	C
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

Truth table 3.3 : 8-3 binary encoder (8 inputs and 3 outputs)

Points to Remember

- Defined as a circuit which translates an **n bit data-word** into a smaller **m-bit code-word**.
- Used to do bit compression.
- Architecture consists of a linear array of m ORing elements.

3.3.5 Counters

A counter is a sequential circuits that counts the **number of incoming clock pulses.** It consists of an array of flip-flops.

Or

In digital logic and computing, a counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal.

In the following sections, negative edge triggered JK flip-flops are used for discussions on the working of the various types of counters.

Basically there are two types of counters. "Parallel counters (or) Synchronous counters" and "Ripple counters (or) Asynchronous counters".

Asynchronous Binary Up Counter: Let us consider a three bit counter for simplicity. It must have a count sequence 000

001...111, as shown in the table below. Q0, Q1, Q2 are outputs of the flip-flops are cleared with a PC RESET input such that Q2Q1Q0=000. Thereafter with every clock, the output increments as shown.

CK	Q2	Q 1	Q ₀
RESET	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0
9	0	0	1
10	0	1	0



Fig. 3.8: Asynchronous Binary Up Counter

After every eight clocks the count sequence repeats itself. From the count sequences table given above it can be seen that Q_0 toggles with every clock. Hence the CK pulse is directly applied to the first flip-flop. But $Q_{(i)}$ toggles whenever $Q_{(i-1)}$ makes a negative transition that is when $Q_{(i-1)}$ changes from 1 to 0. Hence the clocks for subsequent flip-flops are obtained from the $Q_{(i)}$ output of the previous flip-flop.

Note that in an asynchronous counter the J and K inputs are always kept high so that the flip-flop toggles when a clock arrives.

Asynchronous Binary down Counter

A binary down counter counts with every clock and hence it is initially SET with DCSET input.



Fig. 3.9: Asynchronous Binary down Counter

The counter state table is given below. It can be seen from the count sequence table that Q0 toggles with every clock. Hence the first flip-flop is clocked directly. For the other flip-flops $Q_{(i)}$ toggles only when $Q_{(i-1)}$ makes a positive transition. That is when $Q_{(i-1)}$ makes a negative transition. Hence the clocks are derived from the complementary outputs for these flipflops.

For convenience, a three bit natural binary counter is treated in the above discussions.

The same logic can be extended to 4-bit (or) 5-bit counter or an n-bit counter.

Synchronous Binary Counter

In a **synchronous counter**, the flip-flops are all clocked simultaneously. Hence the J and K inputs are made high only when necessary. (Recall that in asynchronous counters, J and K inputs are always high, that is the flip-flops are in toggle mode and when a clock arrives the flip-flop toggles).

CK	Q2	Q1	Q0
RESET	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0
9	0	0	1
10	0	1	0

Truth Table: 3.4: Synchronous Binary Encoder

And so on.

A careful study of the count sequence table will reveal that a flip-flop toggles only when the outputs of the previous flip-flops are high. ie. $Q_{(i)}$ toggles only when $Q_{(i-1)}$ AND $Q_{(i-2)}$ AND $Q_{(i-3)}$... AND $Q_{(0)}=1$.

This fact is made use of in realizing a synchronous counter.

3.4 TYPES OF SEQUENTIAL CIRCUIT

Latches & Flip Flops: latches and flip-flops are the building blocks of sequential circuits both latches and flip-flops are circuit elements whose output depends not only on the current inputs, but also on **previous inputs and outputs.** The difference between a latch and a flip-flop is that a latch does not have a **clock signal**, whereas a flip-flop always does and latches can be built from gates and flip-flops can be built from latches.

A flip flop is a bi **stable device**, that is, it can remain in one of the **two stable states** which are designated as "0" and "1" states. It is the fundamental logic circuit used for storing information in digital systems. Different types of shift registers and counters are designed only using flip flops, which can be built using NOR gates or NAND gates. A flip flop has two outputs, one of which is the complement of the other. They are called Normal and complement outputs.

3.4.1 RS Flip Flop

The RS Flip flop can be implemented in many ways. One such implementation is shown in Figure 3.7 There are two inputs to the RS Flip Flop. These lines are used to control the output of the flip-flop. The working of the flip-flop is as follows:

Case: 1

When S=0 and R=0. Now both the NAND gates A and B output logic 1. Hence the outputs of C and D depend only on the feedback inputs (secondary inputs). The primary inputs, that is outputs of gates A and B are don't cares now. In other words the entire circuit behaves as a latch. Thus the circuit will **"hold on"** to its previous output. This state is called "HOLD" state.



Fig: 3.10:RS Flip Flop

Figure shows an RS Flip Flop constructed with four NAND gates A, B, C and D.

It has two inputs S and R and two outputs Q and Q'. (The state of any flip-flop is known by the state of a output only).

Case: 2

When S=0 and R=1. Now gate A will output 1 and B will output as 0. The output of D

that is Q' will be 1, making both inputs to **gate cas** 0. Hence Q will be in a 1 state. This state of the flip flop is known as "RESET" state.

Case: 3

When S = 1 and R = 1. This input condition is prohibited. This is because when both S and R are equal to 1, gates A and B will output 0', which will force both Q and Q' to 1. This is against the principle of operation of a flip flop. Moreover, if the inputs are now changed, the next state of the flip flop is unpredictable. The next state actually depends on which gate is faster to change its present state. This prohibited state is also called "**RACE**" condition.

Case 4:

When S=1 and R=0. This is just the reverse of case 2. On similar arguments we can see that now Q=1 and Q'=0. This state of the flip-flop is known as "SET" state.

The above stated input output relations are represented below on in truth table.

INP	UTS	OUTPUT	MODE
S	R	Q(N+1)	MODE
0	0	Q(N)	HOLD
0	1	0	RESET
1	0	1	SET
1	1	*	Prohibited

The disadvantages of an RS flip-flops are twofold...

- · Both inputs must be considered when writing the memory
- There is no means of synchronization

3.4.2 D flip flop

In the RS Flip flop the condition R=1 and S=1 is forbidden. This state can be avoided by connecting an inverter between S and R inputs. The flip flop with this modified connection is called a **D** flip flop.

When the clock is 0 and the D input does not affect the output. So when the clock is 0, D is treated as don't care. The value of D is prevented from reading the output until a clock pulse occurs. When the clock is high, both the AND gates are enabled and the value of D appears at Q.

When the clock goes low and last value is retained by Q. This Flip-flop is also called as a **delay Flip**-flop or data flip-flop.



(o) characteristics ra

Fig:3.11: (a) D-Flip-Flop and (b)Truth Table

3.4.3 JK Flip-flop

A flip-flop is a refinement of the SR flip-flop in that the in determinate condition of the SR type is defined in the JK type inputs J and K behave like inputs S and R to set and clear the Flip-flop, respectively. When inputs J and K are both equal to 1, a clock transition switches the outputs of the flip-flop to their complement state.

The graphic symbol and characteristic table of the JK flip-flop are shown in Figure. 3.12.

The J input is equivalent to the S (set) input of the SR flip-flop, and the K input is equivalent to the R (clear) input. Instead of the indeterminate condition, the JK flip-flop has a complement condition Q (t+1) = Q'(t) when both J and K are equal to 1.



J	K	Q(t+1)	
0	0	Q(r)	No change
0	1	0	Clear to 0
1	0	1	Set to 1
1	1	Q'(t)	Complement

Fig:3.12(a) J-K Flip Flop Graphic Symbol &(b) Truth Table

3.4.4 T Flip Flop

Another type of flip flop is the **toggle flip flop.** This flip flop is obtained from a JK flip flop when inputs J and K are connected to provide a single input designated by t. The T flip flop has only two conditions. When T=0 (J=K=0) a clock transition does not change the state of the flip flop. When T=1(J=K=1) a clock transition complements the state of the flip flop.

These conditions can be expressed by a characteristics equation.



Fig 3.13: (a) T-Flip-Flop Graphic Symbol & (b) Truth Table

SUMMARY

Flip-flops are clocked, latches are only enabled. This is an easy way to remember the difference. Flip-flops usually have an enable connection too, so that they may avoid communication on any given clock tick. They offer synchronous communication through use of a shared clock.

"D" is for Data, "T" is for Toggle! "D" is also for Delay since data at the input of a D flip-flop cannot be input to a second one until the following clock tick. A delay is therefore afforded in passing data along

a string of flip-flops of one clock period per device. The JK flip-flop allows a number of different processes to be programmed, some with asynchronous and some with synchronous effect. It may be thought of as the most primitive possible programmable processor.

3.5 REGISTER

A register is simply a **collection of flip-flops** wide enough to contain one complete word of data. Registers are read onto, and written from, a data bus, which is of width equal to that of the registers themselves. Some means must be provided to enable the connection of any one particular register to the bus and to ensure that it either reads or writes the bus but not both simultaneously.

These are basic building blocks for construction of combinational and sequential circuits.

There are following types of register on the basis of Data Transmission:

Serial-in to Parallel-Out (SIPO): the register is loaded with serial data, one bit at a time, with the stored data being available in parallel form.

Serial-in to Serial-Out (SISO): the data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.

Parallel-in to Serial-Out (PISO): the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.

Parallel-in to Parallel-Out (PIPO): the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

The effect of data movement from left to right through a register can be presented graphically as



Fig. 3.14: Graphical Representation of SISD,SIMD,MISD,MIMD

3.5.1 Data Register

The data register is one of the most common components of contemporary computers. Its function, on any clock tick, may be defined by previously setting or clearing the following control inputs...

• R/W (Read/Write)

• En (Enable)

R/W means "read not write" when set and therefore "write not read" when clear or Re-set. It is

standard. An serves to decide whether a read or write operation is to be allowed or not. Remember that, unlike the data inputs, control inputs are asynchronous. They must be set up prior to the clock tick when the operation is required.

3.5.2 Shift Register

The Shift Register is another type of **sequential logic circuit** that is used for the storage or transfer of data in the form of binary numbers and then "shifts" the data out once every clock cycle, hence the name shift register. It basically consists of several single bit "D-Type Data Latches", one for each bit (0 or 1) connected together in a serial or **daisy-chain arrangement** so that the output from one data latch becomes the input of the next latch and so on. The data bits may be fed **in or out** of the register **serially**, i.e. one after the other from either the left or the right direction, or in parallel, i.e. all together. The number of individual data latches required to make up a single Shift Register is determined by the number of bits to be stored with the most common being 8-bits wide, i.e. eight individual data latches.

Applications of Shift Register

Shift Registers are used for data storage or data movement and are used in calculators or computers to store data such as two binary numbers before they are added together, or to convert the data from either a **serial to parallel or parallel to serial format.** The individual data latches that make up a single shift register are all driven by a common clock (Clk) signal making them **synchronous devices.**

The directional movement of the data through a shift register can be either to the left, (left shifting) to the right, (right shifting) left-in but right-out, (rotation) or both left and right shifting within the same register thereby making it bidirectional.

There is following types of shift register:

(a) 4-bit Serial-in to Parallel-out Shift Register: The operation is as follows. Let's assume that all the flip-flops (FFA to FFD) have just been RESET (CLEAR input) and that all the outputs QA to QD are at logic level "0" i.e, no parallel data output. If a logic "1" is connected to the DATA input pin of FFA then on the first clock pulse the output of FFA and therefore the resulting QA will be set HIGH to logic "1" with all the other outputs still remaining LOW at logic "0". Assume now that the DATA input pin of FFA has returned LOW again to logic "0" giving us one data pulse or 0-1-0.



Fig. 3.15: 4-bit Serial-in to Parallel-out Shift Register

The second clock pulse will change the output of FFA to logic "0" and the output of FFB and QB

HIGH to logic "1" as its input D has the logic "1" level on it from QA. The logic "1" has now moved or been "shifted" one place along the register to the right as it is now at QA. When the third clock pulse arrives this logic "1" value moves to the output of FFC (QC) and so on until the arrival of the fifth clock pulse which sets all the outputs QA to QD back again to logic level "0" because the input to FFA has remained constant at logic level "0".

The effect of each clock pulse is to shift the data contents of each stage one place to the right, and this is shown in the following table until the complete data value of 0-0-0-1 is stored in the register. This data value can now be read directly from the outputs of QA to QD. Then the data has been converted from a serial data input signal to a parallel data output. The truth table and following waveforms show the propagation of the logic "1" through the register from **left to right** as follows.

Clock Pulse No	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	0	0	0	0

Basic Movement of Data through a Shift Register



Fig. 3.16: Basic Movement of Data through a Shift Register

Note that after the fourth clock pulse has ended the 4-bits of data (0-0-0-1) are stored in the register and will remain there provided clocking of the register has stopped. In practice the input data to the register may consist of various combinations of logic "1" and "0". Commonly available SIPO IC's include the standard 8-bit 74LS164 or the 74LS594.

Serial-in to Serial-out (SISO)

This shift register is very similar to the SIPO above, except were before the data was read directly in a parallel form from the outputs QA to QD, this time the data is allowed to flow straight through the register and out of the other end. Since there is only one output, the DATA leaves the shift register one bit at a time in a serial pattern, hence the name Serial-in to Serial-Out Shift Register or SISO.

The SISO shift register is one of the simplest of the four configurations as it has only three connections, the serial input (SI) which determines what enters the left hand flip-flop, the serial output (SO) which is taken from the output of the right hand flip-flop and the sequencing clock signal (Clk). The logic circuit diagram below shows a generalized serial-in serial-out shift register.

(b) 4-bit Serial-in to Serial-out Shift Register: You may think what's the point of a SISO shift register if the output data is exactly the same as the input data. Well this type of Shift Register also acts as a temporary storage device or as a time delay device for the data, with the amount of time delay being controlled by the number of stages in the register, 4, 8, 16 etc or by varying the application of the clock pulses.



Fig. 3.17: 4-bit Serial-in to Serial-out Shift Register

Commonly available IC's include the 74HC595 8-bit Serial-in/Serial-out Shift Register all with 3state outputs.

Parallel-in to Serial-out (PISO)

The Parallel-in to Serial-out shift register acts in the **opposite way** to the serial-in to parallel-out one above. The data is loaded into the register in a parallel format i.e. all the data bits enter their inputs simultaneously, to the parallel input pins PA to PD of the register. The data is then read out sequentially in the normal shift-right mode from the register at Q representing the data present at PA to PD. This data is outputted one bit at a time on each clock cycle in a serial format. It is important to note that with this system a clock pulse is not required to parallel load the register as it is already present, but four clock pulses are required to unload the data.



(c) 4-bit Parallel-in to Serial-out Shift Register:

Fig. 3.18: 4-bit Parallel-in to Serial-out Shift Register

As this type of shift register converts parallel data, such as an 8-bit data word into serial format, it can be used to multiplex many different input lines into a single serial DATA stream which can be sent directly to a computer or transmitted over a communications line. Commonly available IC's include the 74HC166 8-bit Parallel-in/Serial-out Shift Registers.

Parallel-in to Parallel-out (PIPO)

The final mode of operation is the Parallel-in to Parallel-out Shift Register. This type of register also acts as a temporary storage device or as a time delay device similar to the SISO configuration above. The data is presented in a parallel format to the parallel input pins PA to PD and then transferred together directly to their respective output pins QA to QA by the same clock pulse. Then one clock pulse loads and unloads the register. This arrangement for parallel loading and unloading is shown below.

4-bit Parallel-in to Parallel-out Shift Register

The PIPO shift register is the simplest of the four configurations as it has only three connections, the parallel input (PI) which determines what enters the flip-flop, the parallel output (PO) and the sequencing clock signal (Clk).



Fig. 3.19: 4-bit Parallel-in to Parallel-out Shift Register

Similar to the Serial-in to Serial-out shift register, this type of register also acts as a temporary storage device or as a time delay device, with the amount of time delay being varied by the frequency of the clock pulses. Also, in this type of register there are no interconnections between the individual flip-flops since no serial shifting of the data is required.

Universal Shift Register

Today, high speed bi-directional "universal" type Shift Registers such as the TTL 74LS194, 74LS195 or the CMOS 4035 are available as a 4-bit multi-function devices that can be used in either serial-to-serial, left shifting, right shifting, serial-to-parallel, parallel-to-serial, and as a parallel-to-parallel multifunction data register, hence the name "Universal". These devices can perform any combination of parallel and serial input to output operations but require additional inputs to specify desired function and to pre-load and reset the device.

4-bit Universal Shift Register 74LS194



Fig. 3.20: 4-bit Universal Shift Register 74LS194

Universal shift registers are very useful digital devices. They can be configured to respond to operations that require some form of temporary memory, delay information such as the SISO or PIPO configuration modes or transfer data from one point to another in either a serial or parallel format. Universal shift registers are frequently used in arithmetic operations to shift data to the left or right for multiplication or division

3.6 ADDER

Digital computers perform a variety of information processing tasks. Among the functions encountered are the various arithmetic operations. The most basic arithmetic operation is the addition of two binary digits. This simple addition consists of four possible elementary operations:

0+0=0, 0+1=1, 1+0=I, and 1+1=10. The first three operations produce a sum of one digit, but when both **augend** and **addend** bits are equal to 1, the binary sum consists of two digits. The higher significant bit of this result is called a **carry**. When the augend and addend numbers contain more significant digits, the carry obtained from the addition of two bits is added to the next higher order pair of significant bits. A combinational circuit that performs the addition of two bits is called a **half-adder**. One that performs the addition of three bits (two significant bits and a previous carry) is a **full adder**. The names of the circuits stem from the fact that two half adders can be employed to implement a full adder.

3.6.1Half Adder

From the verbal explanation of a half adder, we find that this circuit needs two binary inputs and two binary outputs. The input variables designate the augend and addend bits; the output variables produce the sum and carry. We assign symbols x and y to the two iaputs and S (for sum) and C (for carry) to the outputs. The truth table for the half adder is listed in Table 3-7.

The C output is 1 only when both inputs are 1. The S output represents the least significant bit of the sum.

The simplified Boolean functions for the two outputs can be obtained directly from the truth table. The simplified sum of products expressions are

S = x'y + xy'

C = xy

The logic diagram of the half adder implemented a sum of products is shown in Fig. 3.22. It can be also implemented with an exclusive-OR and an AND gate as shown in Fig. 3.22(b).

This form is used to show that two half adders can be used to construct a full adder.

INPUT	SUM OF BITS
0+0	0
0+1	1
1+0	1
1+1	0 With a carry of 1

Table 3.6 Addition Rule in Binary Number System

Input		Outpu	ıt
X	Y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 3.7 Truth Table for Half Adder



Fig. 3.21Block Diagram



Fig. 3.22: Logic Diagram of Half Adder with X-OR & AND Gate (b) with AND & OR Gate

In the half-adder diagram there are two inputs to the half-adder and two outputs. If either of the inputs is a 1 but not both, then the output on the S line will be a 1. If both inputs are 1s, the output on the C line will be a 1. For all other states, there be a 0 output on the carry line. These relationships may be written in Boolean form as follows.

S = XY' + X'YC = XY

3.6.2 Full Adder

The adder circuit is capable of adding the content of two registers. It must include provision for handling carries as well as an addend and augends bits. So there must be **three inputs to each** stage of a multi digit adder, except the stage for the least significant bits. One for each input from the numbers being added, one for any carry that might have been generated or propagated by the previous stage.

There are three inputs to the full-adder X and Y inputs from the respective digits of the registers to be added, the Ci input, which is for any carry generated by the previous stage. The two outputs are S, which is the output value for that stage of the addition, and C0, which produces the carry to be added into the next stage. The Boolean expressions for the input output relationships for each of the **two** outputs are as follows:



Full adder circuit – Block Diagram

Fig. 3.23: Logic Diagram & Truth Table of Full Adder

Truth Table

Points to Remember about Adder

In electronics, an adder or summer is a digital circuit that performs addition of numbers.

In modern computers adders reside in the arithmetic logic unit (ALU) where other operations are performed.

Although adders can be constructed for many numerical representations, such as Binary-coded decimal or excess-3, the most common adders operate on binary numbers.

3.7 GLOSSARY

Combinational logic consists of logic gates and is a type of digital logic which is implemented by boolean circuits, where the output is a pure function of the present input only.

Sequential circuits contain logic gates as well as memory cells. Their outputs depend on the present inputs and also on the states of memory elements. Multiplexer is a combinational logic circuit, which has many inputs and only one output.

Demultiplexer performs a function opposite to that of a multiplexer. It has one data input and several output lines.
Decoder is digital circuit that has several output lines and control input lines. Based on the value of the control input (or select input), one of the output lines will become active.

Encoder is a digital circuit that generates the binary code corresponding to the input number Counter is a sequential circuits that counts the number of incoming clock pulses.

Latches & Flip Flops: latches and flip-flops are the building blocks of sequential circuits both latches and flip-flops are circuit elements whose output depends not only on the current inputs, but also on previous inputs and outputs. The difference between a latch and a flip-flop is that a latch does not have a clock signal, whereas a flip-flop always does and latches can be built from gates and flip-flops can be built from latches.

Register is simply a collection of flip-flops wide enough to contain one complete word of data.

Shift Register is another type of sequential logic circuit that is used for the storage or transfer of data in the form of binary numbers and then "shifts" the data out once every clock cycle.

Half Adder is combinational circuit that performs the addition of two bits is called a half-adder. **Full Adder** is performs the addition of three bits (two significant bits and a previous carry)

3.8 REVIEW QUESTIONS

- Q.1 What are Combinational & Sequential Circuits Differentiates
- Q2 How do we know, if given a circuit, whether it is a Combinational Circuit or a Sequential Circuit?
- Q.3 How you will identify that the circuits is combinational or sequential?
- Q.4 Explain MULTIPLEXER.
- Q.5 Implement an AND gate using multiplexer?
- Q.6 Write about En-coder & De-coder.
- Q.7 Implement D- fillip flip from
 - RS flip flop;
 - Multiplexer.
- **Q.8** Design a 2bit up/down counter with clear using gates.
- Q.9 How full Adder is implemented by TWO Half Adder?
- Q.10 What is the difference between a latch and a flip flop?
- **Q.11** What is the race around condition? How can it be overcome?

Chapter 4

Multilevel View Point of Machine

4.0 OBJECTIVE

This chapter is about the computer organization & architecture. **the purpose of it** is to prepare clear & complete understanding of nature & characteristics of modern computer systems. The main objectives this chapter is as follows:

- Understand the concept of Computer Organization
- Understand the concept of Computer Architecture
- Differences between Organization & Architecture
- · Concept of ISA and Micro-architecture
- Role of High level Languages
- I/O Devices Communication
- Concept of MIPS/MFLOPS/C.P.U Performance
- · Overview of Organizational Structure

4.1 BASICS OF COMPUTER ORGANIZATION & ARCHITECTURE

Computer Organization: refers to the operational units & their interconnections that realize the architectural specifications, Therefore **Computer organization deals with structural relationships that are not visible to the programmer** (like clock frequency or the size of the physical memory).

Computer Architecture or **Digital Computer Organization:** It is referring to those attributes of system that are visible to Programmer. In other words, we can also say that the computer architecture refers to the attributes that have a **direct impact on logical execution of Program** (like the size of a data type - 32 bits to an integer)

OR

It may also be defined as the science and art of selecting and interconnecting hardware components to create computers that meet functional, performance and cost goals

OR

In computer science and computer engineering, computer architecture or digital computer organization is the **conceptual design and fundamental operational structure of a computer system**.

It forms a blueprint and functional description of requirements and design implementations for the various parts of a computer, focusing largely on the way by which the central processing unit (CPU) performs internally and accesses addresses in memory

OR

A different definition of computer architecture is built on Four basic viewpoints:

- (i) Structure,
- (ii) Organization,
- (iii) Implementation, and
- (iv) Performance

In this definition, the **structure** defines the **interconnection** of various hardware components, the **organization** defines the **dynamic interplay and management** of the various components, the **implementation** defines the detailed design of **hardware components**, and the **performance** specifies the **behavior** of the computer system

There is a concept of levels in computer architecture. The basic idea is that there are many levels at which a computer can be considered, from the highest level, where the user is running programs, to the lowest level, consisting of transistors and wires



Fig. 4.1: Levels of Computer Architecture

Computer architecture comprises at least Three main subcategories:

- **Instruction Set Architecture:** or ISA, is the abstract image of a computing system that is seen by a machine language (or assembly language) programmer, including the instruction set, word size, memory address modes, processor registers, and address and data formats.
- **Micro Architecture:** also known as Computer organization is a lower level, more concrete and detailed, description of the system that involves how the constituent parts of the system are interconnected and how they interoperate in order to implement the ISA. The size of a computer's cache for instance, is an organizational issue that generally has nothing to do with the ISA.
- System Design which includes all of the other hardware components within a computing system such as:

- 1. System interconnects such as computer buses and switches
- 2. Memory controllers and hierarchies
- 3. CPU off-load mechanisms such as Direct Memory access (DMA)
- 4. Issues like multiprocessing.

4.2 MICRO-ARCHITECTURE

In computer engineering **micro architecture** (sometimes abbreviated to µarch or uarch), also called computer organization, is the way a given **instruction set architecture** (ISA) is implemented on a processor. A given ISA may be implemented with different micro architectures. Implementations might vary due to different goals of a given design or due to shifts in technology. Computer architecture is the combination of micro-architecture and instruction set design

OR

The Micro-Architecture is the architecture that includes the constituent parts of the processor and how these interconnect and interoperate to implement the ISA.

The micro-architecture of a machine is usually represented as (more or less detailed) diagrams that describe the **interconnections of the various micro architectural elements of the machine**, which may be everything from single gates and registers, to complete arithmetic logic units (ALU)s and even larger elements. These diagrams generally separate the **data path** (where data is placed) and the **control path** (which can be said to steer the data).

Each micro-architectural element is in turn represented by describing the **interconnections of logic gates** used to implement it. Each logic gate is in turn represented by a **circuit diagram** describing the connections of the transistors used to implement it in some particular logic family. Machines with different micro-architectures may have the same instruction set architecture, and thus be capable of executing the same programs. New micro-architectures and/or circuitry solutions, along with advances in semiconductor manufacturing, are allows newer generations of processors to achieve higher performance while using the same ISA.

In principle, a single micro-architecture could execute several different ISAs with only minor changes to the microcode.

4.3 INPUT/OUTPUT

In computing, **input/output, or I/O**, refers to the communication between an information processing system (such as a computer), and the outside world, possibly a human, or another information processing system. Inputs are the signals or data received by the system, and outputs are the signals or data sent from it. The term can also be used as part of an action; to **"perform I/O"** is to perform an input or output operation. I/O devices are used by a person (or other system) to communicate with a computer. For instance, a keyboard or a mouse may be an input device for a computer, while monitors and printers are considered output devices for a computer. Devices for communication between computers, such as modems and network cards, typically serve for both input and output.

Note that the designation of a device as either input or output depends on the perspective. Mouse and keyboards take as input physical movement that the human user outputs and convert it into signals that a computer can understand. The output from these devices is input for the computer. Similarly, printers and monitors take as input signals that a computer outputs. They then convert these signals into representations that human users can see or read. For a human user the process of reading or seeing these representations is receiving input. These interactions between computers and humans is studied in a field called **human-computer interaction**.

In computer architecture, the combination of the CPU and main memory (i.e. memory that the CPU can read and write to directly, with individual instructions) is considered the brain of a computer, and from that point of view any transfer of information from or to that combination, for example to or from a disk drive, is considered I/O. The CPU and its supporting circuitry provide memory-mapped I/O that is used in low-level computer programming in the implementation of device drivers. An I/O algorithm is one designed to exploit locality and perform efficiently when data reside on secondary storage, such as a disk drive.

4.4 HIGH-LEVEL PROGRAMMING LANGUAGE

A high-level programming language is a programming language with strong abstraction from the details of the computer. In comparison to low-level programming languages, it may use natural language elements, be easier to use, or be more portable across platforms. Such languages hide the details of CPU operations such as memory access models and management of scope.

This greater abstraction and hiding of details is generally intended to make the language userfriendly, as it includes concepts from the problem domain instead of those of the machine used. A highlevel language isolates the execution semantics of computer architecture from the specification of the program, making the process of developing a program simpler and more understandable with respect to a low-level language. The amount of abstraction provided defines how "high-level" a programming language is.

The first high-level programming language to be designed for a computer was **Plankalkül**, created by Konrad Zuse. However, it was not implemented in his time and his original contributions were isolated from other developments.

High level language is a language that supports the human and the application sides of the programming (typical features: ability to logic structuring of the algorithm, cross-platform independence, problemoriented syntax/semantic, etc.).

4.4.1 High Level Language Vs Lower Level Language

- The term "high-level language" does not imply that the language is superior to low-level programming languages-in fact, in terms of the depth of knowledge of how computers work required to productively program in a given language, the inverse may be true.
- Rather, "high-level language" refers to the higher level of abstraction from machine language.
- Rather than dealing with registers, memory addresses and call stacks, high-level languages deal with variables, arrays, objects, complex arithmetic or boolean expressions, subroutines and functions, loops,

• Features such as string handling routines, object-oriented language features and file input/output may also be present.

Low level language is a language that supports the machine side of the programming or does not provide human side of the programming (typical features: lack of identifiers, lack of cross-platform independence, full access to the processor architecture, etc.)

4.5 CENTRAL PROCESSING UNIT

The central processing unit (CPU) is the portion of a computer system that carries out the instructions of a computer program, and is the primary element carrying out the functions of the computer or other processing device. The central processing unit carries out each instruction of the program in sequence, to perform the basic arithmetical, logical, and input/output operations of the system. This term has been in use in the computer industry at least since the early 1960s



Fig. 4.2: Computer Processor

4.5.1 The Control Unit

The control unit of the CPU contains circuitry that uses electrical signals to direct the entire computer system to carry out, stored program instructions.

The control unit does not execute program instructions; rather, it directs other parts of the system to do so. The control unit must communicate with both the arithmetic/logic unit and memory.

4.6 MIPS/MFLOPS AND CPU PERFORMANCE

MIPS (Million Instructions Per Second)

It is unfortunate that the term MIPS is used as a processor benchmark as well as a shorthand form of a company name, so first I better make the distinction clear. The company responsible for the CPU designs in the N64 is MTI, an abbreviation for MIPS Technologies Inc

MIPS

The processor benchmark called **MIPS has nothing** to do with the company name. In the context of CPU performance measurement, MIPS stands for '**Million Instructions Per Second'**. The MIPS rating of a CPU refers to **how many low-level machine** code **instructions a processor** can **execute in one second**. Unfortunately, using this number as a way of measuring processor performance is completely pointless because no two chips use exactly the same kind of instructions, execution method, etc. For example: on one chip, a single instruction may do many things when executed (**CISC = Complex Instruction Set Computing**), whereas on another chip a single instruction may do very little but is dealt with more efficiently (RISC = Reduced Instruction **Set** Computing). Also, different instructions on the same chip often do vastly different amounts of work (eg. a simple arithmetic instruction might take just 1 clock cycle to complete, whereas doing something like floating point division or a square root operation might take 20 to 50 clock cycles).

MIPS numbers are often very high because of how processors work, but in fact the number tells one absolutely nothing about **what the processor** can actually do or how it works (ie. a processor with a lower MIPS rating may actually be a better chip because its instructions are doing more work per clock cycle). There are dozens of different processor and system benchmarks, such as SPEC, Linpack, MFLOP, STREAM, Viewperf, etc.An example: imagine a 32bit processor running at 400MHz. It might be rated at 400MIPS. Now consider a 64bit processor running at 200MHz. It might be rated at 200MIPS (assume a simple design in each case). But suppose my task involves 64bit fp processing (eg. computational fluid dynamics, or audio processing, etc.): the 32bit processor would take many more clock cycles to complete a single 64bit fp multiply since its registers are only of a 32bit word length. The 32bit CPU would take at least twice as long to carry out such an operation. Thus, for 64bit operations, the 32bit processor would be much slower than the 64bit processor. Now think of it the other way round: suppose one's task only involved 32bit operations. Unless the 64bit registers in the 64bit CPU could be treated as two 32bit registers, the 32bit CPU would be much faster. It all depends on the processing requirements.

The situation in real life is far more complicated though, because real CPUs rarely do one thing at a time and in just one clock cycle. Simple arithmetic operations may take 1 cycle, an integer multiply might take 2 cycles, a fp multiply might take 5 clock cycles, a complex square root operation in a CISC design take 20 cycles, and so on. Worse, some CPUs are designed to do more than one of the same kind of operation at once, ie. they have more than one of a particular kind of processing unit.

So that's the MIPS benchmark dealt with, ie. it's useless, so ignore it.

MFLOPS

It is popular alternative approach to measure execution time is million floating-point operations per second, or MFLOPS (megaflops). The formula for MFLOPS is simply

 ${\rm MFLOPS} = \frac{{\rm Number \ of \ floating-point \ operations \ in \ a \ program}}{{\rm Execution \ time} \times 10^6}$

MFLOPS is fine, but it misses one very important point: **memory bandwidth.** A fast CPU may sound impressive, and people will always talk in terms of theoretical peak performance, etc., but in

reality a CPU's best possible performance totally depends on the rate at which it can access data from the various kinds of memory (L1 / L2 cache and main RAM). A fast CPU in a system with low memory bandwidth will not perform anywhere near its theoretical peak (eg. 500MHz Alpha).

4.6.1 Using MIPS and MFLOPS as Performance Metrics

To measure CPU performance in MIPS, or million instructions per second. For a given program, MIPS is given by:

 $MIPS = \frac{Instruction \ count}{Execution \ time \times 10^6}$

Since,

Execution time = $\frac{\text{Instruction count} \times \text{CPI}}{\text{Clock rate}}$

Equation 1 becomes

$$IMPS = \frac{Clock rate}{CPI \times 10^6}$$

Since MIPS is a rate of operations per unit time, CPU performance can be specified as the inverse of execution time, with faster machines having a **higher MIPS rating.** How-ever, according to the Patterson and Hennessy, there are problems with using MIPS as a performance metric.

- MIPS is dependent on the instruction set of the CPU, making it difficult to compare the MIPS ratings of processors with different instruction sets.
- MIPS can vary inversely to performance.

Consider the MIPS rating of a processor with an optional floating-point unit. Since it generally takes more clock cycles per floating-point instruction that per integer instruction, floating-point programs using the optional hardware instead of software floating-point routines take less time but have a lower MIPS rating. A software floating-point routine executes simpler instructions, resulting in a higher MIPS rating, but it executes so many more instructions that the overall execution time is longer.

We can see similar anomalies with optimizing compilers as the following example demonstrates.

Example Let us assume that you have profiled your code and the instruction mix is detailed in Table 1. We now want to build an optimizing compiler for the CPU. The compiler discards 50% of the ALU instructions although it cannot reduce loads, stores, or branches.

Assuming a 20-ns clock cycle time (or a 50-MHz clock), what is the MIPS rating for the optimized code versus the un-optimized code? Does the MIPS rating agree with the ranking of execution time?

The optimized code is 13% faster, but its MIPS rating is lower! As this example shows, MIPS can fail to give a true picture of performance in that it does not track execution time.

Operation	frequency	СРІ
ALU Operations	43%	1
Loads	21%	2
Stores	12%	2
Branches	24%	2

Table 4.1 The instruction mix and CPIs of individual instructions

Answer. We use the CPU performance formula to computer the CPI of the unoptim code as

$$CPI_{unoptimized} = .43 \times 1 + .21 \times 2 + .12 \times 2 + .25 \times 2 = 1.57$$

So,

$$\text{MIPS}_{\text{unoptimized}} = \frac{50 \, MHz}{1.5 \times 10^6} = 31.85$$

The performance of the unoptimized code, in terms of execution time, is given by:

 $CUP = Time_{unoptimized} = Instruction Count_{unoptimized} \times 1.57 \times (20 \times 10^{-9})$ $= 31.4 \times 10^{-9} \times Instruction Countu_{noptimized}$

For the optimized code,

$$CPI_{optimized} = \frac{\frac{43}{2} \times 1 + .21 \times 2 + .12 + .24 \times 2}{1 - \frac{.43}{2}}$$
$$= 1.73$$

since 50% of the ALU operations have been discarded (.43/2) and the instruction cow reduced by the missing ALU instruction. Thus,

MIPSoptimized =
$$\frac{50 MHz}{1.73 \times 10^6} = 28.90$$

The performance of the optimized code, in terms of execution time, is

CPU time_{optimized} =
$$(.785 \times \text{Instruction}_{\text{countunoptimized}}) \times 1.73 \times (20 \times 10^{-9})$$

= 27.2 × 10–9 × Instruction count_{unoptimized}

Another popular alternative to measure execution time is million floating-point operations per second, or (MFLOPS) The formula for MFLOPS is simply.

 $MFLOPS = \frac{Number of floating-point operations in a program}{Execution time \times 10^{6}}$

The MFLOPS rating is dependent on the machine and on the program, and since MFLOPS are intended to measure floating-point performance, they are not applicable outside that range. For example, compilers have a MFLOPS rating of nearly zero no matter how fast the CPU is since compilers rarely use floating-point arithmetic. When comparing the performance of different machines, MFLOPS is not dependable because the set of floating-point operations is not consistent across machines.

4.7 ORGANIZATIONAL STRUCTURE

An organizational structure consists of activities such as task allocation, coordination and supervision, which are directed towards the achievement of organizational aims. It can also be considered as the viewing glass or perspective through which individuals see their organization and its environment.

An organization can be structured in many different ways, depending on their objectives. The structure of an organization will determine the modes in which it operates and performs.

Organizational structure allows the expressed allocation of responsibilities for different functions and processes to different entities such as the branch, department, workgroup and individual.

Organizational structure affects organizational action in two big ways. First, it provides the foundation on which standard operating procedures and routines rest. Second, it determines which individuals get to participate in which decision-making processes, and thus to what extent their views shape the organization's actions.

4.7.1 Pre-bureaucratic structures

Pre-bureaucratic (entrepreneurial) structures lack standardization of tasks. This structure is most common in smaller organizations and is best used to solve simple tasks. The structure is totally centralized. The strategic leader makes all key decisions and most communication is done by one on one conversations. It is particularly useful for new (entrepreneurial) business as it enables the founder to control growth and development.

4.7.2 Bureaucratic structures

Weber (1948, p. 214) gives the analogy that "the fully developed bureaucratic mechanism compares with other organizations exactly as does the machine compare with the non-mechanical modes of production. Precision, speed, unambiguity, ... strict subordination, reduction of friction and of material and personal costs- these are raised to the optimum point in the strictly bureaucratic administration." It have a certain degree of standardization. They are better suited for more complex or larger scale organizations.

The Weberian characteristics of bureaucracy are:

· Clear defined roles and responsibilities

- A hierarchical structure
- Respect for merit.

4.7.3 Post-bureaucratic

The term of post bureaucratic is used in two senses in the organizational literature: one generic and one much more specific. In the generic sense the term post bureaucratic is often used to describe a range of ideas developed since the 1980s that specifically contrast themselves with Weber's ideal type bureaucracy. Another smaller group of theorists have developed the theory of the Post-Bureaucratic Organization, provide a detailed discussion which attempts to describe an organization that is fundamentally not bureaucratic. Charles Heckscher has developed an ideal type, the post-bureaucratic organization, in which decisions are based on dialogue and consensus rather than authority and command, the organization is a network rather than a hierarchy, open at the boundaries (in direct contrast to culture management); there is an emphasis on meta-decision making rules rather than decision making rules.

4.7.4 Functional structure

Employees within the functional divisions of an organization tend to perform a specialized set of tasks, for instance the engineering department would be staffed only with software engineers. This leads to operational efficiencies within that group. However it could also lead to a lack of communication between the functional groups within an organization, making the organization slow and inflexible.

As a whole, a functional organization is best suited as a producer of standardized goods and services at large volume and low cost. Coordination and specialization of tasks are centralized in a functional structure, which makes producing a limited amount of products or services efficient and predictable. Moreover, efficiencies can further be realized as functional organizations integrate their activities vertically so that products are sold and distributed quickly and at low cost. For instance, a small business could start making the components it requires for production of its products instead of procuring it from an external organization. But not only beneficial for organization but also for employees faiths.

4.7.5 Divisional structure

Also called a "product structure", the divisional structure groups each organizational function into a division. Each division within a divisional structure contains all the necessary resources and functions within it. Divisions can be categorized from different points of view. One might make distinctions on a geographical basis (a US division and an EU division, for example) or on product/service basis (different products for different customers: households or companies). In another example, an automobile company with a divisional structure might have one division for SUVs, another division for subcompact cars, and another division for sedans.

Each division may have its own sales, engineering and marketing departments.

4.7.6 Matrix structure

The matrix structure groups employees by both function and product. This structure can combine the best of both separate structures. A matrix organization frequently uses teams of employees to accomplish work, in order to take advantage of the strengths, as well as make up for the weaknesses, of functional and decentralized forms. An example would be a company that produces two products, "product a" and "product b". Using the matrix structure, this company would organize functions within the company as follows: "product a" sales department, "product a" customer service department, "product a" accounting, "product b" sales department, "product b" customer service department, "product b" accounting department. Matrix structure is amongst the purest of organizational structures, a simple lattice emulating order and regularity demonstrated in nature.

- Weak/Functional Matrix: A project manager with only limited authority is assigned to oversee the cross- functional aspects of the project. The functional managers maintain control over their resources and project areas.
- **Balanced/Functional Matrix:** A project manager is assigned to oversee the project. Power is shared equally between the project manager and the functional managers. It brings the best aspects of functional and projectized organizations. However, this is the most difficult system to maintain as the sharing power is delicate proposition.
- **Strong/Project Matrix:** A project manager is primarily responsible for the project. Functional managers provide technical expertise and assign resources as needed.

Among these matrixes, there is no best format; implementation success always depends on organization's purpose and function

4.8 GLOSSARY

Computer Organization: refers to the operational units & their interconnections that realize the architectural specifications, ThereforeComputer organization deals with structural relationships that are not visible to the programmer (like clock frequency or the size of the physical memory).

Computer Architecture or Digital Computer Organization: It is referring to those attributes of system that are visible to Programmer. Instruction Set Architecture: or ISA, is the abstract image of a computing system that is seen by a machine language (or assembly language) programmer, including the instruction set, word size, memory address modes, processor registers, and address and data formats.

System Design which includes all of the other hardware components within a computing system

Micro architecture also called computer organization, is the way a given instruction set architecture (ISA) is implemented on a processor

Input/Output, or I/O, refers to the communication between an information processing system (such as a computer), and the outside world, possibly a human, or another information processing system.

High-Level Programming Language is a programming language with strong abstraction from the details of the computer.

MIPS: It is used as a processor benchmark but it is very effective to calculate execution time, it is Million Instructions per Second

MFLOPS It is popular alternative to measure execution time is Million Floating-Point Operations Per Second.

An organizational structure consists of activities such as task allocation, coordination and supervision, which are directed towards the achievement of organizational aims.

4.9 **REVIEW QUESTIONS**

- Q.1 Write about Computer Architecture.
- Q.2 How you could explains differences between Computer Architecture & Organization?
- Q.3 What is an ISA, Differentiate between ISA Micro-architecture?
- Q.4 How High Level Languages are useful in design of computer?
- Q.5 Write about MIPS and MFLOPS.
- Q.6 Discuss Organizational Structure.

UNIT-II

Chapter 5

Instruction Set Architecture

5.0 OBJECTIVE

After going through this chapter you should able to:

- · Describe the characteristics of Instruction set
- · Discussion of various elements of instruction
- ISAs Classification- CISC, RISC
- · Operations on Instruction Set

5.1 INTRODUCTION

Instruction set architecture is part of processor that is visible to the programmer **or** compiler designer. They are the parts of processor design that needed to understand in order to write assembly language such as machine language instructions & registers. The ISAs serve as boundary between Hardware & Software.

5.2 WHAT IS ISA

An Instruction Set is a set of programming instructions, which allow a computer system to carry about commands necessary for operation

OR

An instruction set, or instruction set architecture (ISA), is the part of the computer architecture related to programming, including the native data types, instructions, registers, addressing modes, memory architecture, interrupt & exception handling, and external I/O.

OR

Instruction set architecture is part of processor that is visible to programmer or complier designer. These are part of processor design that needed to be understood in order to write assembly language, such as machine language instructions and registers.

OR

Instruction set is **collection of machine language instructions** that are a particular processor understands and executes, In other words in ISA A set of assembly language mnemonic represents the machine code of particular computer, therefore if we define all instructions of computer, we can say that we have defined the INSTRUCTION SET. Instruction set architecture is distinguished from the micro-architecture, which is the set of processor design techniques used to implement the instruction set. Computers with different micro-architectures can share a common instruction set architecture(ISA). For example, the **Intel Pentium** and the **AMD Athlon** implement nearly identical versions of the **x86** instruction set, but have radically different internal designs.

This concept can be extended to unique ISAs like TIMI (Technology-Independent Machine Interface) present in the **IBM System/38** and **IBM AS/400.** TIMI is an ISA that is implemented by low-level software translating TIMI code into "native" machine code, and functionally resembles that is now referred to as a virtual machine. It was designed to increase the longevity of the platform and applications written for it, allowing the entire platform to be moved to very different hardware **without having to** modify any software except that which translates TIMI into native machine code, and the code that **implements services used by the resulting native code.** This allowed IBM to move the AS/400 platform from an older CISC architecture to the newer POWER architecture **without having to rewrite or recompile any parts of the OS or software associated with it other than the aforementioned low-level code.** Some virtual machines that support bytecode for Smalltalk, the Java virtual machine, and Microsoft's Common Language Runtime virtual machine as their ISA implement it by translating the **bytecode** for commonly used code paths into native machine code, and executing less-frequently-used code paths by interpretation.

Facts to Know:

It should be noted that instructions available in a computer are machine dependent that is the different processors have different instruction sets

A instruction set can have different Instruction format, the instruction format represent:

- (a) The instruction length
- (b) The type
- (c) Length and position of operation code in instruction and
- (d) The number and length of operand addresses etc.

5.3 WHAT ARE THE ELEMENTS OF AN INSTRUCTION?

Each instruction have several fields the most common fields of instruction format are

OPCODE(What operation to perform): An operation code filed terms as opcode that specifies the operation **to be performed.**

Or

The opcode field of an instruction is group of bits that define various processor operations such as LOAD, STORE, ADD and SHIFT to be performed on some data stored in the register or in memory.

OPERANDS: An address field of operand on which data processing to be performed. The operand can reside in the memory or a processor register or can be incorporated within the operand field of instruction as immediate constant, Therefore a mode field is needed that specifies the way the operand or its address to be determined.

A sample instruction format is given as:



Fig. 5.1: Instruction format of 32 Bits

Please note the following points from the Figure

- The opcode size is 6 bits, therefore in general it has $2^6 = 3^2$ operations (However instruction designer develop much more operations)
- There is only one operand address machine
- There are two bits for addressing modes, therefore there are $2^2 = 4$ different addressing modes possible for this machine

Last field (8-31 bits=24) here is operand or address of operand field

- In case of immediate operand the maximum size of unsigned operand or address the maximum size of unsigned operator would be 2^{24}
- In case of an address of operand in the memory, then maximum physical memory size supported by machine is $2^{24} = 16MB$
- The Opcode field of an instruction is a group of bits that define the various processor operations such as LOAD, ADD and SHIFT to be perform on same data stored in register or memory
- The operand address field can be data ,or can refer to data-that is address of data or can be labels which may be address of instruction you want to execute next, An operand address can be:
 - Memory Address
 - CPU register address
 - I/O device address
- An ISA includes a specification of the set of opcodes (machine language), and the native commands implemented by a particular processor.

Points to Remember:

- 1. The ISA is the interface between the software and hardware.
- 2. It is the set of instructions that bridges the gap between high level languages and the hardware.
- 3. For a processor to understand a command, it should be in **binary** and not in High Level Language. The ISA encodes these values.
- 4. The ISA also defines the items in the computer that are available to a programmer. For example, it defines data types, registers, addressing modes, memory organization etc.
- 5. Register are high Addressing modes are the ways in which the instructions locate their operands.

5.4 CLASSIFICATION OF INSTRUCTION SET ARCHITECTURE

There are many computer architecture classification methods based on different criteria such as cost, capacity (memory size, data word length and size of the secondary storage), performance, instruction set, component base and others. On the basis of Instruction Set computer architectures can be classified into **Two** Categories:

(i) COMPLEX INSTRUCTION SET COMPUTER (CISC)

(ii) REDUCED INSTRUCTION SET COMPUTER (RISC)

The processor we will be considering in this book is the **MIPS processor**. The MIPS processor, designed in 1984 by researchers at Stanford University, is a RISC (Reduced Instruction Set Computer) processor. Compared with their CISC (Complex Instruction Set Computer) counterparts (such as the Intel Pentium processors), RISC processors typically support **fewer and much simpler instructions**.

5.4.1 COMPLEX INSTRUCTION SET COMPUTER (CISC)

CISC, which stands for Complex Instruction Set Computer, is a philosophy for designing chips that are **easy to program and which make efficient use of memory.** Each instruction in a CISC instruction set might perform a series of operations inside the processor. This reduces the number of instructions required to implement a given program, and allows the programmer to learn a small but flexible set of instructions.

Since the earliest machines were programmed in assembly language and memory was slow and expensive, the CISC philosophy made sense, and was commonly implemented in such large computers as the PDP-11 and the DECsystem.

Most common microprocessor designs-- including the Intel(R) 80x86 and Motorola 68K series-also follow the CISC philosophy.

CISC:Use Microcode

The earliest processor designs used dedicated **hardwired logic to** decode and execute each instruction. That was appropriate for simple designs with few registers, but made architectures more complex and hard to build. Developers of computer systems took another approach; they built simple logic to control the data paths between the various elements of the processor, and used **microcode instruction set to control the data path logic.** In those systems, the main processor has some built-in ROM, which contains groups of microcode instructions, corresponding to each machine-language instruction (a macrocode instruction).

Because instructions could be retrieved much faster from a local ROM than from main memory, designers put as many instructions as possible into microcode. Microcode implementation allows using the same programming model among different hardware configurations, beside the advantage of easily modifying the instruction set. Some machines were optimized for scientific computing, others were optimized for business computing; however, since they all shared the same instruction set, programs could be moved from one machine to another without re-compilation (but with a possible increase or decrease in performance depending on the underlying hardware.) This kind of flexibility and power made micro-coding the preferred way to build new computers for some time.

This type of implementation is known as a **micro-programmed implementation**. In a microprogrammed system, the main processor has some built-in memory (typically ROM) which contains groups of microcode instructions which correspond with each machine-language instruction. When a machine language instruction arrives at the central processor, the processor executes the corresponding series of microcode instructions.

Because instructions could be retrieved up to **10 times faster from a local ROM** than from main memory, designers began to put as many instructions as possible into microcode. There are some real advantages to a micro-coded implementation:

- since the microcode memory can be much faster than main memory, an instruction set can be implemented in microcode without losing much speed over a purely hardwired implementation.
- new chips are easier to implement and require fewer transistors than implementing the same instruction set with dedicated logic

CISC:Build"rich"instruction sets

One of the consequences of using a micro-programmed design is that designers could build more functionality into each instruction. This not only cut down on the total number of instructions required to implement a program, and therefore made more efficient use of a slow main memory, but it also made the assembly-language programmer's life simpler.

Soon, designers were enhancing their instruction sets with instructions aimed specifically at the assembly language programmer. Such enhancements included string manipulation operations, special looping constructs, and special addressing modes for indexing through tables in memory.

For example:

ABCD Add Decimal with Extend ADD AAdd Address ADD XAdd with Extend ASL Arithmetic Shift Left CAS Compare and Swap Operands NBCD Negate Decimal with Extend EORI Logical Exclusive OR Immediate TAS Test Operand and Set **CISC:** Build high-level Instruction sets

Once designers started building programmer-friendly instruction sets, the logical next step was to build instruction sets which map directly from high-level languages. Not only does this simplify the compiler writer's task, but it also allows compilers to emit fewer instructions per line of source code.

Modern CISC microprocessors, such as the 68000, implement several such instructions, including routines for creating and removing stack frames with a single call.

For example:

DBcc Test Condition, Decrement and Branch ROXL Rotate with Extend Left RTR Returnand Restore Codes SBCD Subtract Decimal with Extend SWAP Swap register Words

CMP2 Compare Register against Upper and Lower Bounds

The rise of CISC

CISC Design Decisions:

Use micro code

build rich instruction sets

buildhigh-level instruction sets

Taken together, these three decisions led to the CISC philosophy which drove all

computer designs until the late 1980s, and is still in major use today

Disadvantages of CISC

CISC philosophy had its own problems, including:

- Earlier generations of a processor family generally were contained as a subset in every new version --- so instruction set & chip hardware become more complex with each generation of computers.
- So that as many instructions as possible could be stored in memory with the least possible wasted space, individual instructions could be of almost any length---this means that different instructions will take different amounts of clock time to execute, slowing down the overall performance of the machine.
- Many specialized instructions aren't used frequently enough to justify their existence --- approximately **20%** of the available instructions are used in a typical program.
- CISC instructions typically set the condition codes as a side effect of the instruction. Not only does setting the condition codes take time, but programmers have to remember to examine the condition code bits before a subsequent instruction changes them.
- Complex instruction decoding scheme, an increased size of the control unit, and increased logic delays.

Points to Remember about CISC architecture

- Many different formats are possible For example the DEC VAX architecture supplies addressing modes which auto-increment or auto-decrement an array index after, or before, carrying out an operation.
- · 2-operand format, register to memory and memory to register instructions,
- multiple addressing modes for memory,
- · variable length instructions and many clock cycles per instruction
- The result is a complex processor executing instructions rather more slowly than its RISC
- CISC Large instruction set to suit broad range of applications
- Number of instructions are reduced by having multiple operations within a single instruction
- Multiple operations lead to many different kinds of instructions that access memory
- In turn making instruction length variable and fetch-decode execute time unpredictable making it more complex

- hardware handles the complexity(Hardwired Organization)
- CISC architecture Use less instructions to execute same code is executed by RISC but instructions are complicated
- Instruction Set: large set of instruction with variable size (16 to 64)
- Addressing Modes: 12-24
- General Purpose registers: 8-24
- Clock rate: 33-50MHz in 1992
- A CISC system has complex instructions such as direct addition between data in two memory locations.Eg.8085 Motivations for complexity.
- The motivations towards complexity are largely due to attempts to continue the upgrading of existing, successful products. They may be summarized...
- Speed up specified application operations via hardware implementation
- · Reduce semantic gap via hardware implementation of programming language statements
- · Maintain upwards compatibility in product line
- · Reduce size of machine code software because of high memory cost

5.4.2 Risc(Reduced Instruction Set Computer)

RISC started as a notion in the 1980s and has eventually led to the development of the first RISC machine, the IBM 801 minicomputer, real-life manifestation appeared in the **Berkeley RISC-I and the Stanford MIPS machines**, which were introduced in the mid-1980s. The launching of the RISC notion announces the start of a new paradigm in the design of computer architectures. This **paradigm promotes simplicity in computer architecture design**.

The Complex Instruction Set has a number of disadvantages, These include a complex instruction decoding scheme, an increased size of the control unit, and increased logic delays. These drawbacks prompted a team of computer architects to adopt the principle of "less is actually more" RISC processors implement small instruction sets capable of running faster than CISC instructions.

RISC Characteristics

The essential goal of RISC architecture involves an attempt to reduce execution time by simplifying the instruction set of the computer. The major characteristics of a RISC processor are:

- · Relatively few instructions.
- · Relatively few addressing modes.
- Instruction Set:Small set of instruction with fixed size (32-bit)
- Addressing Modes: 3-5
- General Purpose registers: 32-192
- Clock rate: 50-150MHz in 1993
- load store architecture used
- pipelining can be implemented easily.Eg.ATMELAVR
- Memory access limited to load and store instructions.

- Hardwired rather than micro programmed control.
- Single-cycle instruction execution This objective could only be achieved by pipelining Small instruction set, Load/store architecture Fixed length coding and hardware decoding, Delayed branching and one clock per instruction.
- The phases in the execution path are typically: instruction fetch, decoding, operand fetch, execution, memory access and write back of the operation results.
- The whole benefit of a RISC architecture can be defeated if the compiler is not sophisticated enough to rearrange instructions in the optimal order
- RISC architectures try to maximize the cooperation between hardware and software.
- Optimizing compilers are one of the essential components of RISC systems. This act of shifting the burden of code optimization from the hardware to the compiler was one of the key advances of the RISC revolution.
- RISC processors depend on a complex memory hierarchy in order to work at full speed.
- RISC Processors can be classified according to many measures that affect the performance, like the word size, data path width, pipeline depth, cache structure as split versus common or on-chip versus off-chip, bus structure as Harvard versus Princeton, pre fetch buffers and write buffers, register files as common versus private, register management as score boarding versus register renaming and units chaining capability.

A typical RISC processor architecture includes **register-to-register operations**, with only simple load and store operations for memory access.

Thus the operand is code into a processor register with a load instruction. All computational tasks are performed among the data stored in processor registers and with the help of store instructions results are transferred to the memory. This architectural feature simplifies the instruction set and encourages the optimization of register manipulation. Almost all instructions have simple register addressing so only a few addressing modes are utilised. Other addressing modes may be included, such as **immediate operands** and **relative mode**.

An advantage of RISC instruction format is that it is easy to decode.

An important feature of RISC processor is its ability to execute one instruction per clock cycle. This is done by a procedure referred to as pipelining. A load or store instruction may need two clock cycles because access to memory consumes more time than register operations. Other characteristics attributed to RISC architecture are:

- A relatively large number of register in the processor unit.
- Use of overlapped register windows to speed-up procedure call and return.
- Efficient instruction pipeline.
- Compiler support for efficient translation of high-level language programs into machine language programs.

5.5 CISC/RISC DESIGN ISSUES

The design of the instruction set for the processor is very important in terms of computer architecture. It's the instruction set of a particular computer that determines the way that machine language programs are constructed. Computer hardware is improvised by various factors, such as upgrading existing models to provide more customer applications adding instructions that facilitate the translation from high-level language into machine language programs and striving to develop machines that move functions from software implementation into hardware implementation. A computer with a large number of instructions is classified as a complex instruction set computer, abbreviated as CISC.

An important aspect of computer architecture is the design of the instruction set for the processor, some of points are discussed here:-

- The instruction set determines the way that machine language programs are constructed
- Many computers have instructions sets of about 100 250 instructions
- These computers employ a variety of data types and a large number of addressing modes complex instruction set computer (CISC)
- A RISC uses fewer instructions with simple constructs so they can be executed much faster within the CPU without having to use memory as often
- The essential goal of a CISC architecture is to attempt to provide a single
- machine instruction for each statement that is written in a high-level language
- The goal of RISC architecture is to reduce execution time by simplifying the instructions set

5.6 RISC VERSUS CISC

Many of the techniques used in RISC processors can be implemented in **CISC designs.** It is possible to rewire the processor in order to execute most of the instructions in one cycle, or it is possible to use a pipelined micro engine in order to speed up execution. The micro engine could be a RISC kernel giving all the advantages of RISC without its disadvantages. However, RISC features can be introduced in CISC processors only at the expense of much more hardware. It is possible to program the pipeline of a CISC processor to use the dead time between the load and store of one instruction argument in memory. The micro engine works in this case following a load/store model, and it dynamically reschedules the operations needed by the macrocode. This dynamical rescheduling is too expensive compared to the software scheduling used in RISC processors. Software scheduling must be done only once and then it runs without complex hardware. Dynamic scheduling needs much more hardware logic.

CISC designers move complexity from software to hardware, making tradeoffs in favor of decreased code size, at the expense of a higher cycle per seconds (CPI). While RISC designers move complexity from hardware to software, making tradeoffs in favor of a lower CPI, at the expense of increased code size. CISC processors can still be made competitive to RISC processors if the cycle time is reduced, but RISC processors are better positioned to achieve greater reductions in the clock cycle time in the long run. The cycle time is determined by the following factors: pipelining depth, amount of logic in each stage and the VLSI technology used. RISC processors can achieve larger reductions in the clock cycle time with a lower investment in design time. Reducing the clock cycle time of CISC processors is possible, but much more difficult. The question is which design philosophy will be capable of climbing

5.7 COMPARISON OF RISC AND CISC

Closure of the semantic gap and applications support look very good in the catalogue and have proved popular. However, once the CISC machine language is implemented, an application may not run faster than it would on a RISC. The reasons are twofold. Firstly, the powerful instructions take time to translate into a sequence of primitive operations. Secondly, all that CISC complexity could have been exchanged for a larger register file, to gain greater benefit from locality, or even for another separate processor. The latter would reap benefit if parallelism exists at the problem level and hence at the algorithmic level.

To summarize, the advantages of RISC are improvements in...

- Performance for structured software via exploitation of temporal locality
- Reliability and freedom from design errors
- Design and development path
- Compiler/architecture interface

Those factors which a CISC maintains in its favour are...

- Code length
- Application specific performance
- Upwards compatibility with older machines

It must be emphasized that RISC machines demonstrate several innovations. Each must be considered separately. Research is still under way to discover which truly offer the greatest rewards. The reader is strongly encouraged to read [Colwell et al. 85] for an up-to-date account of these matters.

Although there is great controversy over the RISC vs CISC issue, several new machines are now available visibly benefiting from RISC architecture. These include the Acorn Archimedes, SUN 4 and IBM RT. The only arguable disadvantages to a RISC are that the size of object module is increased and that programming at machine level is slightly more work. It is not harder work since the machine language is simpler. Neither of these is of great importance to someone whose primary concern is performance and who programs in a high level language (as most do).

Apart from an uncompetitive performance, CISC has a more serious disadvantage. The design and development paths are **long and risky.** By the time some have reached the market they are almost out of date. The cost of development is high and rapidly rising. The greater complexity also impacts reliability. By contrast the development of RISC designs is short and cheap. For example the Acorn ARM processor was developed on a very short time scale and the very first chip made was reported to function perfectly. It was designed on an Acorn home micro using their own software. The cost and reliability of the chip set make it very competitive. Designing optimized code generators for a RISC is generally easier than for a CISC. Part of the motivation behind the RISC concept is that existing compilers were not making sufficient use of complex instructions.

Let us examine relative advantages & disadvantages of RISC and CISC architecture of processor with a suitable example

The simplest way to examine the advantages and disadvantages of RISC architecture is by contrasting it with it's predecessor: CISC (Complex Instruction Set Computers) architecture

Multiplying Two Numbers in Memory

On the right is a diagram representing the storage scheme for a generic computer. The main memory is divided into locations numbered from (row) 1: (column) 1 to (row) 6: (column) 4. The execution unit is responsible for carrying out all computations. However, the execution unit can only operate on data that has been loaded into one of the six registers (A, B, C, D, E, or F). Let's say we want to find the product of two numbers - one stored in location 2:3 and another stored in location 5:2 - and then store the product back in the location 2:3.



Fig: 5.2 Multiplication of two number

The CISC Approach

The primary goal of CISC architecture is to complete a task in as few lines of assembly as possible. This is achieved by building processor hardware that is capable of understanding and executing a series of operations. For this particular task, a CISC processor would come prepared with a specific instruction (we'll call it "MULT"). When executed, this instruction loads the two values into separate registers, multiplies the operands in the execution unit, and then stores the product in the appropriate register. Thus, the entire task of multiplying two numbers can be completed with one instruction:

MULT 2:3, 5:2

MULT is what is known as a "complex instruction." It operates directly on the computer's memory banks and does not require the programmer to explicitly call any loading or storing functions. It closely resembles a command in a higher level language. For instance, if we let "a" represent the value of 2:3 and "b" represent the value of 5:2, then this command is identical to the C statement "a = a * b."

One of the primary advantages of this system is that the compiler has to do very little work to translate a high-level language statement into assembly. Because the length of the code is relatively short, very little RAM is required to store instructions. The emphasis is put on building complex instructions directly into the hardware.

The RISC Approach

RISC processors only use simple instructions that can be executed within one clock cycle. Thus, the "MULT" command described above could be divided into three separate commands: "LOAD," which moves data from the memory bank to a register, "PROD," which finds the product of two operands located within the registers, and "STORE," which moves data from a register to the memory banks. In order to perform the exact series of steps described in the CISC approach, a programmer would need to code four lines of assembly:

LOAD A, 2:3 LOAD B, 5:2 PROD A, B STORE 2:3, A

At first, this may seem like a much less efficient way of completing the operation. Because there are more lines of code, more RAM is needed to store the assembly level instructions. The compiler must also perform more work to convert a high-level language statement into code of this form.

CISC	RISC	
1. Emphasis on hardware	Emphasis on software	
2. Includes multi-clock	single-clock,	
3. complex instructions	reduced instruction only	
4. Memory-to-memory:	Register to register:	
"LOAD" and "STORE"		
5. incorporated in instructions	"LOAD" and "STORE"	
are independent instructions		
6. Small code sizes,	Low cycles per second,	
7. high cycles per second	Large code sizes	
8. Transistors used for storing	Spends more transistors	
complex instructions	on memory registers	

However, the RISC strategy also brings some very important advantages. Because each instruction requires only one clock cycle to execute, the entire program will execute in approximately the same amount of time as the multi-cycle "MULT" command. These RISC "reduced instructions" require less

transistors of hardware space than the complex instructions, leaving more room for general purpose registers. Because all of the instructions execute in a uniform amount of time (i.e. one clock), pipelining is possible.

Separating the "LOAD" and "STORE" instructions actually reduces the amount of work that the computer must perform. After a CISC-style "MULT" command is executed, the processor automatically erases the registers. If one of the operands needs to be used for another computation, the processor must re-load the data from the memory bank into a register. In RISC, the operand will remain in the register until another value is loaded in its place.

The Performance Equation

The following equation is commonly used for expressing a computer's performance ability:



The CISC approach attempts to **minimize the number of instructions per program, sacrificing the number of cycles per instruction.** RISC does the opposite, reducing the cycles per instruction at the cost of the number of instructions per program.

RISC Roadblocks

Despite the advantages of RISC based processing, RISC chips took over a decade to gain a foothold in the commercial world. This was largely due to a lack of software support.

Although Apple's Power Macintosh line featured RISC-based chips and Windows NT was RISC compatible, Windows 3.1 and Windows 95 were designed with CISC processors in mind. Many companies were unwilling to take a chance with the emerging RISC technology. Without commercial interest, processor developers were unable to manufacture RISC chips in large enough volumes to make their price competitive.

Another major setback was the presence of Intel. Although their CISC chips were becoming increasingly unwieldy and difficult to develop, Intel had the resources to plow through development and produce powerful processors. Although RISC chips might surpass Intel's efforts in specific areas, the differences were not great enough to persuade buyers to change technologies.

The Overall RISC Advantage

Today, the Intel x86 is arguable the only chip which retains CISC architecture. This is primarily due to advancements in other areas of computer technology. The price of RAM has decreased dramatically. In 1977, 1MB of DRAM cost about \$5,000. By 1994, the same amount of memory cost only \$6 (when adjusted for inflation). Compiler technology has also become more sophisticated, so that the RISC use of RAM and emphasis on software has become ideal.

EXAMPLE 2:

Example for RISC vs. CISC

Consider the program fragments:

				mov ax, 0 mov bx, 10
CISC	mov ax, 10 mov bx, 5 mol bx, ax	RISC	Begin	mov ax, 5 add ax, bx loop Begin

The total clock cycles for the CISC version might be: (2 move × 1 cycle) + (1 mul × 30 cycles) = 32 cycles

While the clock cycles for the RISC version is: (3 Move × 1 cycle) + (5 adds × 1 cycle) + (5 loops × 1 cycle) = 13 cycles

Fig: 5.3: Comparison of operations in CISC/RISC

5.8 INTRODUCTION TO SOME OTHER IMPORTANT INSTRUCTION SET ARCHITECTURES

Besides CISC, RISC following instruction set architecture are implemented in computer organization:-Very Long Instruction Word or VLIW: is a special kind of a self drained pipelined scalar CPU architecture which is closely related to "Explicitly Parallel Instruction Computing" concepts and is specifically designed to take advantage of instruction level parallelism (ILP) which is a methodology to perform and measure the multiple simultaneous operations in a computer program. The VLIW is a typical compiler based instruction set architecture where the computing operations in parallel are accomplished based on a fixed schedule determined when programs are compiled, therefore the processor is not burdened to schedule the computing operations as the responsibility of the scalability and the computing operations lies more with the compiler. Most of the VLIW based CPUs are primarily suitable as embedded media processors which have applications in the consumer electronic devices. Some of the examples of the current VLIW CPUs include the TriMedia media processors by NXP (previously Philips Semiconductors), the SHARC DSP by Analog Devices, the C6000 DSP family by Texas Instruments, and the ST Microelectronics ST200 family (based on the Lx architecture) etc.

MISC (Minimal Instruction Set Computer): is a Instruction Set Architecture which is generally more of stack based rather than depending upon registers and that has a very limited number of basic operations and corresponding opcodes. Being stack based, the MISC has a reduced size of operand specifies where most of the instructions operate on the top most stack entries. The MISC enables a smaller and faster instruction decode unit, therefore facilitating overall faster operation of the individual instructions. The MISC normally lacks on instruction-level parallelism because of the inherent sequential dependencies of the instructions in the architecture. One well known example of the MISC based Instruction Set Architecture is INMOS transputer, designed by a british semiconductor company, INMOS Inc. based in Bristol. The transputer or Transistor computer was one of the first general purpose microprocessors designed specifically to be used in parallel processing computing systems. Some examples of the other instruction sets architectures which are very similar to the MISC are Forth, a structured imperative stack-based and procedure oriented computer programming language, and JVM (Java Virtual

Machine) which conceptually represents the instruction set architecture of a stack-oriented capability architecture using a form of computer intermediate language, commonly referred to as Java bytecode.

EPIC (Explicitly Parallel Instruction Computing): Explicitly Parallel Instruction Computing (EPIC) is an Instruction Set Architecture which is similar to a form of "Very Long Instruction Word" (VLIW) architecture in principle, where one instruction word contains multiple instructions. The EPIC architecture is based on the explicit instruction-level parallelism, which is compiler based at the decision level to decide upon the type of the instructions to be executed in parallel. Unlike the VLIW instruction sets, the EPIC are backward compatible between implementations. The EPIC ISA has been used while development of Intel's IA-64 architecture by Intel and HP. The Itanium and Itanium 2 line of server processors from Intel implement the EPIC ISA.

Vector Processor: Vector processor is an Instruction Set Architecture which enables the CPU to run mathematical operations on multiple data elements simultaneously. The Vector processors pipeline the instructions as well as the data itself as a batch in the CPU mamory thereby reducing the processing latency. The Vector processor is mainly used in the supercomputers or high-end machines such as modern video game consoles, consumer computer video graphics hardware etc.

SISD (Single Instruction, Single Data stream) Single Instruction, Single Data (SISD) refers to an Instruction Set Architecture in which a single processor (one CPU) executes exactly one instruction stream at a time and also fetches or stores one item of data at a time to operate on data stored in a single memory unit .Most of the CPU design, based on the von Neumann architecture, from the beginning till recent times are based on the SISD. The SISD model is a typical non-pipelined architecture with the general-purpose registers, as well as dedicated special registers such as the Program Counter (PC), the Instruction Register (IR), Memory Address Registers (MAR) and Memory Data Registers (MDR).

Single Instruction, Multiple Data (SIMD): is an Instruction Set Architecture that have a single control unit (CU) and more than one processing element (PE) that operates like a von Neumann machine by executing a single instruction stream over PEs, handled through the CU. The CU generates the control signals for all of the PEs and by which executes the same operation on different data streams. The SIMD architecture, in effect, is capable of achieving data level parallelism just like with vector processor. Some of the examples of the SIMD based systems include IBM's AltiVec and SPE for PowerPC, HP's PA-RISC Multimedia Acceleration eXtensions (MAX), Intel's MMX and iwMMXt, SSE, SSE2, SSE3 and SSSE3, AMD's 3DNow! etc.

MISD (Multiple Instructions, Single Data Stream): is an Instruction Set Architecture for parallel computing where many functional units perform different operations by executing different instructions on the same data set. This type of architecture is common mainly in the fault-tolerant computers executing the same instructions redundantly in order to detect and mask errors.

MIMD(**Multiple Instruction**, **Multiple Data Streams**): Multiple Instruction stream, Multiple Data stream (MIMD) is an Instruction Set Architecture for parallel computing that is typical of the computers with multiprocessors. Using the MIMD, each processor in a multiprocessor system can execute asynchronously different set of the instructions independently on the different set of data elements. The MIMD based computer systems can used the shared memory in a memory pool or work using distributed memory across heterogeneous network computers in a distributed environment. The MIMD architectures is primarily used in a number of application areas such as computer-aided design/computer-aided manufacturing, simulation, modeling, communication switches etc.

Orthogonal Instruction Set: is an Instruction Set Architecture where any instruction can use data

of any type via any of the addressing mode without restrictions on the type of registers to be used, thereby working on a very limited set on operational codes and addressing modes. Most of the CISC based computers generally also follow the orthogonal instruction set where an instruction could access either registers or computer main memory, generally in various different ways. Examples of some other computer systems following the Orthogonal instruction set are PDP-11, VAX-11 etc.

5.9 GLOSSARY

INSTRUCTION SET: is a set of programming instructions, which allow a computer system to carry about commands necessary for operation

INSTRUCTION SET ARCHITECTURE (ISA): is the part of the computer architecture related to programming,

OPCODE: operation code filed that specifies the operation to be performed.

OPERANDS: An address field of operand on which data processing to be performed.

CISC: COMPLEX INSTRUCTION SET COMPUTER

RISC: REDUCED INSTRUCTION SET COMPUTER

5.10 REVIEW QUESTIONS

Q.1 List the reasons of increased complexity in ISA?

- Q.2 What are the problems in CISC which encourage the development of RISC.
- **Q.3** Differentiate between:
 - (a) RISC vs CISC
 - (b) Hardwired Vs Micro programmed
 - (c) Opcode vs Operand
- Q.4 What do you understand by Instruction set Architecture? Discuss various designing issues instruction format.
- Q.5 What is load-store architecture Explain?
- **Q.6** Fill in the Blank:
 - (i) ISA stands for_____.
 - (ii) CISC_____
 - (iii) RISC_____
 - (iv) MIPS_____
 - (v) SISD_____
 - (vi) SIMD_____
 - (vii) MISD_____
 - (viii) MIMD_____
 - (ix) EPIC_____
 - (x) MAR_____
 - (xi) MDR_____

Chapter 6

Addressing Modes & Instructions

6.0 OBJECTIVES

- Identify the various types of ISAs on the basis of Addresses in Instruction Sets,
- · Identify the various types of ISAs on the basis of Instructions
- · Instruction Set and Format Design Issues
- Instruction Set: Operations
- · Major Systems Acquisition Manual

6.1 ADDRESSING MODES

The various addressing modes that are defined in a given instruction set architecture define how machine language instructions in that architecture identify the operand (or operands) of each instruction. An addressing mode specifies how to calculate the **effective memory address** of an operand by using information held in registers and/or constants contained within a machine instruction or elsewhere. Many of the instructions which a computer actually executes during the running of a program concern the movement of data to and from memory. It is not possible simply to specify fixed addresses within each instruction, as this would require the location of data to be known at the time when the program was written. This is not possible due to following for several reasons.

- When a program is read from disk, it will be put in memory in a position which cannot be predicted in advance. Hence, the location of any data in the program cannot be known in advance.
- Similarly, data which has been previously archived to files on disk or tape will be loaded into memory at a position which cannot be known in advance.
- If the data we wish to use will be read from an input device, then we cannot know in advance where in memory it will be stored.
- Many calculations involve performing the same operation repeatedly on a large quantity of data (for example, modifying an image which consists of over a million pixels). If each instruction operated on a fixed memory location, then the program would have to contain the same instruction many times, once for each pixel.

We therefore need different strategies for specifying the location of data. Description of addressing mode or scheme is given below:-

6.1.1 Immediate addressing

- The data itself, rather than an address, is given as the operand(s) of the instruction.
- In this mode operand is the data in the operand field of instruction
- · No address field at all, therefore no additional memory access required



Fig. 6:1: Immediate Addressing

• This address mode is used to initialize the value of a variable

• Advantage of this mode is no **additional memory** is required for executing the instruction **Example:** LOAD IMMEDIATE 7 : is actual the value 7 that put into the CPU register

6.1.2 Direct or absolute addressing

- A fixed address is specified.
- In this mode operand field of instruction specifies the direct address of the intended operand
- · Provide limited address space
- · The effective address in this scheme is defined as address of operand
- · Only one memory reference is required to fetch the operand



Fig. 6.2: Direct Addressing Mode

Example if the instruction LOAD 500 uses direct addressing ,then it will result in loading of contents the of memory cell 500 to into CPU register In this example memory cell 500 contain 7 as in diagram then value 7 will be loaded to CPU register

6.1.3 Implied addressing

The location of the data is implied by the instruction itself, so no operands need to be given. For example, a computer might have the instruction INCA, increment the accumulator.

6.1.4 Relative addressing

The location of the data is specified relative to the current value of the program Counter. This is useful for specifying the location of data which is given as part of the program.

6.1.5 Indirect addressing

In this mode of addressing the operand field of instruction specifies the address of the intended operand Example: if instruction LOAD I 500 uses indirect addressing scheme and contain the value 50A and memory location 50 A contains 7 then the value 7 will loaded in to the CPU register



Fig. 6.3: Indirect Addressing

6.1.5 Indexed addressing

In this mode of addressing the operand field of instruction contains an address and index register, which contain the offset . in this mode generally address is used to address the consecutive locations of memory (which store the elements of array) .the index register is special CPU register that contain the indexed value .Index register is used to iterative applications therefore vale of index register incremented or decremented



Fig. 6.4: Indexed Addressing

The location of the data is calculated as the sum of an address specified by one of the previous methods, and the value of an index register. This allows an array of data (for example, an image) to be accessed repeatedly by the same sequence of instructions.

Points to Remember

- The addressing mode specifies a rule for interpreting or modifying the address field of the instruction before the operand is actually referenced
- The decoding step in the instruction cycle determines the operation to be performed, the addressing mode of the instruction, and the location of the operands
- Two addressing modes require no address fields the Implied mode and Immediate mode
- **Implied Mode:** the operands are specified implicitly in the definition of the instruction complement accumulator or zero-address instructions
- Immediate Mode: the operand is specified in the instruction
- Register Mode: the operands are in registers
- **RegisterIndirect Mode:** the instruction specifies a register that contains the address of the operand
- Auto Increment or Auto Decrement Mode: similar to the register indirect mode
- · Direct Address Mode: the operand is located at the specified address given
- Indirect Address Mode: the address specifies the effective address of the operand
- Relative Address Mode: the effective address is the summation of the address field and the content of the PC
- Indexed Addressing Mode: the effective address is the summation of an index register and the address field
- Base Register Address Mode: the effective address is the summation of a base register and the address field



Fig: 6.5 Numerical Example of Addressing Modes

Addressing Mode	Effective Address	Content of AC
Direct address	500	800
Immediate operand	201	500
Indirect address	800	300
Relative address	702	325
Indexed address	600	900
Register		400
Register indirect	400	700
Autoincrement	400	700
Authdecrement	399	450

Fig. 6.6: Tabular list of Numerical Example

Addressing mode	Meaning	Usage
Register	R4 ← R4 + R3	Register based operations
Immediate	R4 ← R4 + 3	Register constant operations
Displacement	R4 ← R4 + M[100+R1]	Local variable accesses.
Register indirect	$R4 \leftarrow R4 + M[R1]$	Pointer based indexing.
Indexed	$R4 \leftarrow R4 + M[R1 + R3]$	Possible application to array indexing.
Direct or absolute	R4 ← R4 + M[201]	Compile time static data indexing.
Memory indirect	$\mathbf{R4} \leftarrow \mathbf{R4} + [\mathbf{M}[\mathbf{M}[\mathbf{R1}]]$	Pointer based indexing.
Autoincrement	$R4 \leftarrow R4 + M[R1]$	Sequential stepping through arrays within a
	R1 ← R1 + d	loop. 'd' represents the step size.
Autodecrement	R1 ← R1 – d	Might also be appropriate for mimicking
	$R4 \leftarrow R4 + M[R1]$	stacks.
Scaled	$R4 \leftarrow R4 + M[100 + R1]$	Array indexing.
	+ R2 * d]	

Table 6.0: Typical Addressing Mode

In general not all of above modes are used for all applications. However some of the common areas where compilers of HLL use them are as:-

<i>Table 0.1: Summary of various adaressing Mode</i>	Table 6.1	: Summary	of various	addressing	Modes
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Addressing Mode	Possible Use
Immediate	For moving and initialisation of variables
Direct	Used for global variables & less often for local variables
Register	Frequently used for storing local variables of procedure
Register indirect	For holding pointers to structure in programming languages C
Index	To access member of an Array
Auto-index mode	For pushing or popping the parameter of procedure
Base register	Employed to re-locate the program in the memory specially in multi programming
Index	Accessing iterative local variables such as array
Stack	Used for local variables
Relative addressing	The location of the data is specified relative to the current value of the program Counter
Implied	The location of the data is implied by the instruction itself, so no operands need to be given

6.2 INSTRUCTIONS

Computer instructions are translation of high level language code to machine level language programs. Thus these point of view instructions can be classified under the following categories



Fig. 6.7: Types of Instructions

- There are Four main categories of computer instructions:
 - Data Transfer
 - Data Manipulation
 - Program Control
 - Miscellaneous/Privileged

6.2.1 Data Transfer Instructions

Transfer data from one location to another without changing the binary information content. The most common transfers are between :

- (i) Processor register and Memory
- (ii) Processor register and I/O
- (iii) Processor Register themselves
- (iv) These instructions need:
 - (a) The location of source & destination operands and
 - (b) The mode of addressing for each operand

Below list of some instruction are given as:-

Load (LD) : Load the contents from memory to register

Input (IN): Transfer the contents from input devices

Store (ST): Store the information from register to memory location

Output (OUT): Transfer the contents from output devices

Move (MOV): Data transfer from register to another or between the CPU register and memory

Push (PUSH): Transfer data from a processor register to top of memory stack

Exchange (XCH): Swap the information between the two registers or a register and memory word **Pop** (POP): Transfer data from top of stack to processor register

Set(SET): Causes the specified operand to be replace by 1s

Clear(CLEAR): Causes the specified operand to be replace by 1s

- Some assembly language conventions modify the mnemonic symbol to differentiate between addressing modes
 - LDI load immediate

Table: 6.2: Eight Addressing Modes for Load Instructions

Mode	Assembly Convention	Register Transfer
Direct address	LDADR	$AC \leftarrow M(ADR)$
Indirect address	LD@ADR	$AC \leftarrow M[M[ADR]]$
Relative address	LD SADR	$AC \leftarrow M[PC + ADR]$
Immediate operand	LD#NBR	$AC \leftarrow NBR$
Index addressing	LD ADR (X)	$AC \leftarrow M[ADR + KR]$
Register	LD R1	$AC \leftarrow R2$
Register indirect	LD (R1)	$AC \leftarrow M[R]$
Autoincrement	LD (R1)+	$AC \leftarrow M[M1], R1 + 1$

6.2.2 Data Manipulation Instructions/Data Processing Instructions

perform arithmetic, logic, and/or shift operation

- Arithmetic instructions:
 - Increment INC
 - Divide DIV
 - Decrement DEC
 - Add w/carry ADDC
 - Add ADD
 - Sub. w/borrow SUBB
 - Subtract SUB
 - Negate (2's comp) NEG
 - Multiply MUL
- · Some computers have different instructions depending upon the data type
 - ADDI Add two binary integer numbers
 - ADDF Add two floating point numbers
 - ADDD Add two decimal numbers in BCD
- Logical and bit manipulation instructions:
 - Clear CLR Clear carry CLRC
 - Complement COM Set carry SETC
 - AND AND Comp. carry COMC

- OR OR Enable inter. EI
- Exclusive-OR XOR Disable inter. DI
- Clear selected bits AND instruction
- Set selected bits OR instruction
- Complement selected bits XOR instruction

EXAMPLE

Logical AND, OR, NOT, XOR operate on binary data stored in the registers if two register contains the data:

R1 = 10110111

```
R2 = 11110000
```

Then,

R1 AND R2 = 10110000, thus AND operation is used as mask that selects certain bits in a word and zeros out the remaining bits

- Shift instructions
 - Logical shift right SHR
 - Rotate right ROR
 - Logical shift left SHL
 - Rotate left ROL
 - Arithmetic shift right SHRA
 - ROR thru carry RORC
 - Arithmetic shift left SHLA
 - ROL thru carry ROLC

Example: logical shifts LOGICAL SHIFT LEFT and LOGICAL SHIFT RIGHT inserts the ZEROS to end bit position and other bits of a word are shifted **left or right respectively.**



Fig:6.8: Logical Shift

6.2.3 Program Control Instructions

- Provide decision-making capabilities and change the program path
- Typically, the program counter is incremented during the fetch phase to the location of the next instruction
- A program control type of instruction may change the address value in the program counter and cause the flow of control to be altered
- This provides control over the flow of program execution and a capability for branching to different program segments
 - Branch (BR): may conditional or unconditional used for implement of loops
 - Return RET: used for RETurning from subprogram
 - Jump (JMP): unconditional branch is used to implement simple loops
 - Compare (CMP): is used to compare two or more sequence or variables
 - Skip (SKP): zero address instruction and used to skip the next instruction to be execute in the sequence
 - Test TST: used for test the condition
 - Call (CALL): used for CALLing subprogram
 - TST and CMP cause branches based upon four status bits: C, S, Z, and V

Mnemonic	Branch condition	Tested condition
BZ	Branch if zero	Z = 1
BNZ	Branch if not zero	$\mathbf{Z} = 0$
BC	Branch if carry	C = 1
BNC	Branch if no carry	C = 0
BP	Branch if plus	S = 0
BM	Branch if minus	S = 1
BV	Branch if overflow	$\mathbf{V} = 1$
BNV	Branch if no overflow	$\mathbf{V} = 0$
	Unsigned compare conditions $(A - B)$	
BHI	Branch if higher	A > B
BHE	Branch if higher or equal	A≥B
BLO	Branch if lower	A < B
BLOE	Branch if lower or equal	$A \leq B$
BE	Branch if equal	A-B
BNE	Branch if not equal	A≠B
	Signed compare conditions $(A - B)$	
BGT	Branch if greater than	A > B
BGE	Branch if greater or equal	$A \ge B$
BLT	Branch if less than	A < B
BLE	Branch if less of qual	$A \leq B$
BE	Branch if equal	A≠B
BNE	Branch if not equal	A=B

Table: 6.3: Conditional Branch Instructions

Table describe some important opcodes categories:

- The first 4 categories are universally supported.
- The latter 4 categories are application dependent

Table: 6.4: instruction Categories

Operator Type	Instance
Arithmetic/Logical	+,-, ×, + (integer)
Data Transfer	Load, Store
Control	Branch, jump, procedure call and return
System	Operating system call, virtual memory management.
Floating Point	+,-, ×, ÷ (FP)
Decimal	+, ×, decimal to character conversion
String	Move, compare, search
Graphics	Pixel and vertex operations, (de)compress operations

6.3 MISCELLANEOUS/PRIVILEGE

These instructions do not fit in any of above categories.

I/O instructions: start I/O, stop I/O, test I/O

Interrupt & state swapping Instructions

Most of computer instructions are divided into **TWO categories**, **Privileged** and **Non-Privileged** A processor running in privileged mode can be execute all **instructions from the instruction set** while a processor is running in user mode can execute only a **sub set of instructions I/O** instructions are example of privileged while clock, interrupt are another one

Some Important points to Remember

- A call subroutine instruction consists of an operation code together with an address that specifies the beginning of the subroutine
 - Execution of CALL:
 - Temporarily store return address
 - Transfer control to the beginning of the subroutine update PC

 $SP \leftarrow \PP - 1$

 $M[SP] \leftarrow PC$

 $PC \leftarrow effective address$

- Execution of RET:
- Transfer return address from the temporary location to the PC

 $PC \leftarrow M[SP]$

 $SP \leftarrow SP + 1$

- **Program Interrupt:** refers to the transfer of program control to a service routine as a result of interrupt request
- Control : returns to the original program after the service program is executed
- An interrupt procedure is similar to a subroutine call except:
 - The interrupt is usually initiated by an internal or external signal rather than an instruction
 - The address of the interrupt service routine is determined by the hardware rather than the address field of an instruction
 - All information necessary to define the state of the CPU is stored rather than just the return address
- The interrupted program should resume exactly as if nothing had happened
- The state of the CPU at the end of the execute cycle is determined from:
 - The content of the PC
 - The content of all processor registers
 - The content of certain status conditions
- The program status word (PSW) is a register that holds the status and controlflag conditions
- Not all computers store the register contents when responding to an interrupt
- · The CPU does not respond to an interrupt until the end of an instruction execution
- The control checks for any interrupt signals before entering the next fetch phase
- Three types of interrupts:
 - External interrupts
 - Internal interrupts
 - Software interrupts
- External interrupts come from I/O devices, timing devices, or any other external source
- Internal interrupts arise from illegal or erroneous use of an instruction or data, also called traps
- · Internal interrupts are synchronous while external ones are asynchronous
- Both are initiated from signals that occur in the hardware of the CPU
- A software interrupt is initiated by executing an Instruction Register, (MDR) and Memory Address Register (MAR). The MDR and MAR are used exclusively by the CPU and are not directly accessible to programmers.
- In order to perform a write operation into a specified memory location, the MDR and MAR are used as follows:
 - The word to be stored into the memory location is first loaded by the CPU into MDR.
 - The address of the location into which the word is to be stored is loaded by the CPU into a MAR.
 - A write signal is issued by the CPU.
- Similarly, to perform a memory read operation, the MDR and MAR are used as follows:
 - The address of the location from which the word is to be read is loaded into the MAR.

6.4 INSTRUCTION SET AND FORMAT DESIGN ISSUES

Some of the basic issues of concerns for instruction set design are:

Completeness: for initial design, primary concern is that the instruction set should be complete which means there is no missing functionality that is it should instructions for basic operations that can be used for creating any possible execution and control operation

Orthogonal: The secondary concern is that the instructions be orthogonal, that is not un-necessary redundant

Instruction Length: it is significant issue of formet design, determine size of instrument **Significance:** It is basic issue of format design, it determines the richness and flexibility of machine Basic Tardeoff: smaller instruction(less space) verse desire more powerful instruction repertoire **Normally programmer desire:-**

- (a) More opcodes and operands: as it result in smaller programs
- (b) More addressing modes: for greater flexibility in implementing function like table manipulations, multiple branching

• Following factors must be considered for deciding about the instruction length:-

Memory Size: if larger range is to be addressed, then more bits may required in address field

Memory Organization: if addressed field is virtual memory then the memory range which is addressed by the instruction is larger than physical memory size

Memory Transfer Length: instructions should be equal to data bus length or multiple of it

Memory Transfer: The data transfer rate from the memory ideally should be equivalent to processor speed, to do it one approach is use to cache memory, second one is to keep instruction to short

Example of Instruction Format

MIPS-2000: it is microprocessor developed by MIPS computer systems in 1990. It have five stage CPU pipe line



Fig:6.9: Pipeline

Note from the Fig:

- All stages are distinct & independent, means the second stage of execution of instruction 1 should not hider instruction 2
- · Over all efficiency of system becomes better

The MOPIS architecture contain 32 bits the instruction format is given below:

Table 6.5: A sample instruction format of MIPS Instruction

ор	rs	rt	rd	shamt	funct
6 Bits	5-Bits	5-Bits	5-Bits	5-Bits	5-Bits

Meaning: op opcodes

rs: first register source operand

rt: second register source operand

rd: destination register operand, store the result

shmat: used in case of shift operation

funct: select the specific variant of operation

6.5 INSTRUCTION SET: OPERATIONS

Multiple Instruction, Single Data (MISD) is an Instruction Set Architecture for parallel computing where many functional units perform different operations by executing different instructions on the same data set. This type of architecture is common mainly in the fault-tolerant computers executing the same instructions redundantly in order to detect and mask errors.

NEON technology: is a set of 128-bit SIMD (single instruction, multiple data) media processing extensions that provides standardized acceleration for next-generation media and signal processing applications. It features a comprehensive instruction set, separate register file and independent execution hardware. NEON technology supports 8-, 16-, 32- and 64-bit integer, and single precision floating-point, SIMD operations for handling audio/video processing as well as graphics and gaming processing. The RealView Development Suite Professional contains the state-of-the-art vectorizing NEON compiler that generates NEON instructions from standard C or C++. This can increase the performance of applications by 400 percent.

6.6 MAJOR SYSTEMS ACQUISITION MANUAL (MSAM)

Major Systems Acquisition Manual (MSAM) defines the **policy** and **process** for major systems acquisition projects. Detailed procedures are provided for applying a uniform and disciplined approach to acquisition planning and project management from mission analysis and requirements generation through design, development, production, and deployment

6.6.1 Major Systems Acquisition Management

It provides definitions of acquisition categories, acquisition phases, and principal decision milestones.



Fig. 6.10: Management Interfaces

Project Managers (PMs) are required to integrate the three primary management areas shown in Figure 6.9 Management Interfaces into a coherent strategy to achieve specificcost, schedule, and performance parameters for their assigned projects.

Requirements Management is the "Sponsor and Technical Authority managed" process with the Sponsor defining mission needs and translating them into sponsor requirements and the Technical Authority ensuring proper Coast Guard technical standards and resources are incorporated. **Business planning** will identify the deficiencies (gaps) that exist between current Coast Guard functional capabilities and the required capabilities of current or projected missions. The **sponsor** is responsible for developing a Mission Need Statement (MNS), derived from business planning activities that describes specific functional capabilities required to accomplish Coast Guard missions that can only be met with materiel solutions. The sponsor is responsible for developing a Concept of Operations (CONOPS) that describes a proposed asset, system or capability in terms of the user needs it will fulfill; the environment in which it will operate; its relationship to existing assets or systems; and the ways it will be used.

6.6.2 Major Systems Acquisition Process Structure

The overall acquisition lifecycle is composed of a pre-acquisition phase (Project Identification) and four distinct acquisition phases: Need; Analyze/Select; Obtain; and Produce/Deploy/Support.



Fig. 6.11 Major Systems Acquisition Life Cycle Framework

The major systems acquisition life cycle is intended to be flexible and may be tailored, with the ADA's approval, to meet the specific circumstances of each acquisition project.

The sponsor identifies and refines specific asset or systems requirements and articulates them in the Operational Requirements Document (ORD).

Major System Acquisition Management is the "Project Manager-owned" process of planning project activities and organizing a project staff to achieve cost, schedule, and performance requirements identified in the ORD and funded in the budget.

Capital Investment Planning is the planning, programming, budgeting, and execution process that is a calendar-driven budgetary process and owned by the Assistant Commandant for Resources (CG-8). Capital investment planning has two interdependent functions - **providing project budget planning** (for funding and personnel) and **establishing affordability constraints.** Project resource planning and management is coordinated by the PM in collaboration with the Sponsor, Technical Authorities and the Commandant (CG-8) staff.

6.7 MODELING AND SIMULATION

A model is a representation of a system, entity, phenomenon, or process that can be used in an experimental environment to gain a better understanding of the system that it is designed to represent. Models can be **physical** (e.g., scale model aircraft for wind tunnel testing), **logical** (process or flow charts) or **mathematical** (e.g., a mathematical model of a specific system created to conduct computer simulations).

Simulation is an exercise of a model (or experiment on the model) over time. It is used to learn specific characteristics about the system that has been built or being built without having to go through expensive testing on the real system or having to wait for real systems to test. Simulations can also be used with real-world systems to replicate a specific environment of operations. One advantage of simulations over real-life is that simulations can be repeated, consistently, any number of times to provide a set of identical tests to a model or real world system.

6.7.1 Msam Using Simulation

It provides vision, policy, procedures, and standards for the administration and management of systems. Major objectives for the use of models and simulation in acquisition are to reduce time, resources, and risk associated with the entire acquisition process, and to increase the quality, military worth, and supportability of fielded systems.

Project Managers and Sponsors are to identify and fund necessary of resources in the early phases of each project to support cost effective analysis of their respective acquisition activities.

6.8 GLOSSARY

ADDRESSING MODES: specifies how to calculate the effective memory address of an operand by using information held in registers and/or constants contained within a machine instruction or elsewhere

IMMEDIATE ADDRESSING: data itself, rather than an address, is given as the operand(s) of the instruction

DIRECT OR ABSOLUTE ADDRESSING: A fixed address is specified

IMPLIED ADDRESSING: location of the data is implied by the instruction itself, so no operands need to be given.

RELATIVE ADDRESSING: location of the data is specified relative to the current value of the program counter.

INDIRECT ADDRESSING: A memory location is given which holds another memory location. This second memory location holds the actual data.

INDEXED ADDRESSING: The location of the data is calculated as the sum of an address specified by one of the previous methods, and the value of an index register

DATA TRANSFER INSTRUCTIONS: transfer data from one location to another without changing the binary information content

DATA MANIPULATION INSTRUCTIONS: perform arithmetic, logic, and/or shift operation PROGRAM CONTROL INSTRUCTIONS: Provide decision-making capabilities and change the program path

MSAM: Major Systems Acquisition Manual

SIMD: Single Instruction, Multiple Data Stream

VLIW :Very Long Instruction Word

MISC: Minimal Instruction Set Computer

EPIC: Explicitly Parallel Instruction Computing

SISD: Single Instruction, Single Data stream

MISD: Multiple Instructions, Single Data stream

MIMD: Multiple Instruction, Multiple Data stream

6.9 REVIEW QUESTIONS

Q.1 Categorize the following operations with Respective Instruction Type

- (a) MOV
- (b) DIV
- (c) STORE
- (d) XOR
- (e) BRN
- (f) COMPARE
- (g) TRAP

Q.2 Discuss the following Addressing Modes:-

- (a) Immediate Addressing
- (b) Direct Addressing
- (c) In-direct Addressing
- (d) Register Indirect Addressing
- (e) Stack Addressing

Q.3 Differentiate between:

(a) SISD Vs SIMD

- (b) Data Processing Instruction vs Data Control Instructions
- (c) Opcode vs Operand
- **Q.5** What do you understand by Instruction set Architecture? Discuss various designing issues instruction format.
- Q.6 What is load-store architecture Explain?

Q.7 State True and False

- (i) Instruction set is collection of all instructions a CPU can execute
- (ii) Instruction can take different format
- (iii) Immediate addressing is best suited for initialization of variables
- (iv) Memory access is faster than register access
- (v) A machine can use most one addressing schemes/modes
- (vi) Long instruction execute faster than short instruction
- 8. Discuss the various elements of Instructions.

9. Explain the concept of MSAM? Discuss process structure.

10 Differentiate between Model and Simulation.

ANSWERS

(ii) True

(iii) False

(iv) False

(i) True (v) False

(vi) False

UNIT-III

Chapter 7

Central Processing Architecture and Data Path

7.0 OBJECTIVE

After going through this chapter you should able to understand the concepts of:

- CPU Architecture types (accumulator, register, stack, memory/ register)
- Detailed data path of a typical register based CPU,
- Fetch-Decode-Execute cycle (typically 3 to 5 stage);
- Microinstruction sequencing,
- Implementation of control unit,
- · Performance Enhancement with pipelining.
- Hardwired control design method,
- Micro Programmed Control Unit.

7.1 INTRODUCTION

A computer system may typically be broken down into a number of components called **devices**, each of which implements, or cooperates in implementing, one or other system function. A minimum of one device is required to implement each function devices must be able to communicate with each other. The form of communication channel employed is the **bus**.

7.2 CPU ARCHITECTURE

A CPU may have following Two types of Architecture

- (i) Non-Pipelined
- (ii) Pipelined

Pipe-lined Architecture:- In pipelined architecture of computers and other digital electronic devices to increase their instruction throughput (the number of instructions that can be executed in a unit of time). The fundamental idea in this architecture is to split the processing of a computer instruction into a **series of independent steps, with storage at the end of each step.** A pipelined architecture consists of following features:-

- The function/interconnection modules are cascadable to form a pipelined processor
- Programmable to do every wanted computation.
- · Synchronization is done using a clock-signal
- The clock signal can control the customizing inputs of the various function/interconnection modules.
- In Each cycle, only one of the modules is needed, so the other modules can simply be disabled, by using low-level customizing inputs.

How Pipe-lined processor Works

Modern CPUs are driven by a clock. The CPU consists internally of logic and register (flip flops). When the clock signal arrives, the flip flops take their new value and the logic then requires a period of time to decode the new values. Then the next clock pulse arrives and the flip flops again take their new values, and so on. By breaking the logic into smaller pieces and inserting flip flops between the pieces of logic, the delay before the logic gives valid outputs is reduced. In this way the clock period can be reduced.

For example, the classic **RISC pipeline** is broken into **five stages** with a set of flip flops between each stage.

- 1. Instruction fetch
- 2. Instruction decode and register fetch
- 3. Execute
- 4. Memory access
- 5. Register write back

Instr. No.		Pipeline Stage					
1	IF	ID	EX	МЕЙ	WB		
2		IF	ID	EX	MEM	WB	
3			IF	ID	EX	MEM	WB
4				IF	ID	EX	MEM
5					IF	ID	EX
Clock Cycle	1	2	3	12	5	6	7

Fig. 7.1: RISC Pipeline: I clock; Instruction Fetch(IF), II Clock: Instruction Decode and Register Fetch(ID)III clock: Execute(EX), IV clock: Memory access, (MEM) and V clock: Register write back(WB)

Processors with pipelining are organized inside into stages which can semi-independently work on separate jobs. Each stage is organized and linked into a **'chain'** so each stage's output is fed to another stage until the job is done. This organization of the processor allows overall processing time to be significantly reduced.

A Deeper Pipeline means that there are more stages in the pipeline, and therefore, **Fewer Logic Gates in Each Stage.** This generally means that the processor's frequency can be increased as the cycle time is lowered. This happens because there are fewer components in each stage of the pipeline, so the propagation delay is decreased for the overall stage.

Non-Pipelined Architecture : In this architecture of CPU instructions are executed **Serially**, and CPU doesn't supply clock to entire circuit, therefore it is supposed that the waveform will be relatively stable and circuit will be low power. This CPU uses **Asynchronous architecture** therefore it needs complete-detection. Some other characteristics feature of Non-Pipelined architecture are given below:-

- A non-pipelined processor executes only a single instruction at a time.
- This architecture prevents branch delays and problems with serial instructions being executed concurrently.
- design is simpler and cheaper to manufacture.
- The instruction latency in a non-pipelined processor is slightly lower than in a pipelined equivalent. This is because extra flip flops must be added to the data path of a pipelined processor.
- A non-pipelined processor will have a stable instruction bandwidth.

Pipelined Vs Non Pipelined

Pipelining enables us to be **executing many instructions at the same time**. Therefore it allows execution to be done in fewer cycles while In Non-pipelined one instruction is executed at a time. When one instruction is completed the next is executed, therefore it is slower

• A non-pipeline architecture is inefficient because some CPU components (modules) are **idle** while another module is active during the instruction cycle while Pipelining **does not completely cancel out idle time in a CPU** but making those modules work in parallel improves program execution significantly

Example

Let's assume that each execution stage in the processor requires a single clock cycle. Figure 7.1 uses a grid to represent a six-stage non-pipelined processor, when instruction [I-1] has finished stage S6, instruction [I-2] begins.

Twelve clock cycles are required to execute the two instructions. In other words, for k execution stages, n instructions require (n * k) cycles to process.

Of course, Figure 7.2 represents a major waste of CPU resources because each stage is used only one-sixth of the time.

	S1	S2	S3	S4	S5	S6
1	I-1					
2		I-1				
3			I-1			
4				I-1		
5					I-1	
6						I-1
7	I-2					
8		I-2				
9			I-2			
10				I-2		
11					I-2	
12						I-2

Fig. 7.2: Non-Piped line execution of Instruction I-1 & I-2

If, on the other hand, a processor supports pipelining, as in Figure 7.2, a new instruction can enter stage S1 during the second clock cycle. Meanwhile, the first instruction has entered stage S2. This enables the overlapped execution of the two in struction s. Two instructions, [I-1] and [I-2], are shown progressing through the pipeline. [I-2] enters stage S1 as soon as [I-1] has moved to stage S2. As a result, only seven clock cycles are required to execute the two instructions.

	S1	S2	S3	S4	S5	S6
1	I-1					
2	I-2	I-1				
3		I-2	I-1			
4			I-2	I-1		
5				I-2	I-1	
6					I-2	I-1
7						I-2
8						
9						
10						
11						
12						

When the pipeline is full, all six stages are in use all the time.

Fig. 7.3: Pipe- lined Execution of Instruction I-1 & I-2

In general, for k execution stages, n instructions require k + (n - 1) cycles to process. Whereas the non-pipelined processor we showed earlier required 12 cycles to process 2 instructions, the pipelined processor can process 7 instructions in the same amount of time.

7.3 ORGANIZATION OF CPU

A typical CPU organization has following Three major components:

- (1) Register set,
- (2) Arithmetic logic unit (ALU), and
- (3) Control unit (CU)

7.3.1 Register Set

The instruction execution takes place in the CPU registers. The register set differs from one computer architecture to another. It is usually a combination of **Two Types** of register set

- (a) General-purpose Register or Processor Register:-General-purpose registers are used for any purpose, hence the name general purpose. A general purpose of register has following characteristics:-
 - In computer architecture, a **processor register** (or **general purpose register**) is a small amount of storage available on the CPU whose contents can be accessed more quickly than storage available elsewhere.
 - Typically, this specialized storage is not considered part of the normal memory range for the machine.
 - Most, but not all, modern computers adopt the **Load-Store Architecture**. Under this architecture, data is loaded from some larger memory be it cache or RAM into registers, manipulated or tested in some way (using machine instructions for arithmetic/logic/comparison) and then stored back into memory, possibly at some different location.
 - Processor registers are at the top of the memory hierarchy, and provide the fastest way for a CPU to access data.
 - General purpose registers are used to store data temporarily either **8 bit data** or **4 bit data** according to their size. Example: B,C,D,E,H,L in 8085
- (b) Special Purpose Register:-Special-purpose registers have specific functions within the CPU. For example; the program counter (PC) is a special-purpose register that is used to hold the address of the instruction to be executed next. Another example of special-purpose registers is the instruction register (IR), which is used to hold the instruction that is currently executed. The ALU provides the circuitry needed to perform the arithmetic, logical and shift operations demanded of the instruction set.

Difference between General Purpose Register & Special Purpose Register

• General purpose is responsible for any type of data so long as it is necessary to be hold by the register. It ranges from **12-32** while Special purpose register is a temporary memory that holds specific data during processing by the processor.

- General purpose registers are used to store **data temporarily either 8 bit data or 4 bit** data according to their size whereas special registers is used for holding the results of **any arithmetic or logic operations carried out** by the arithmetic logic unit
- A special register is the most valuable register that is use for store the large scale data in the memory at a time. So we can easily manage the data as per requirement.
- General purpose registers are used to store temporary data. Example B,C,D,E,H,L in 8085 on the other hand special purpose registers hold the program state. Example Stack pointer(SP),Program Counter(PC) etc.
- General purpose registers are used by **programmer** to store data where as the **special purpose** registers are used by CPU for temporary storage of the data for calculations and other purposes.
- General purpose registers are symmetric and interchangeable and the special purpose registers are symmetric not interchangeable.

Categories of registers

Registers are normally measured by **the number of bits they can hold**, for example, an "8bit register" or a "32-bit register". A processor often contains several kinds of registers, that can be classified accordingly to their content or instructions that operate on them:

- User-Accessible Registers The most common division of user-accessible registers is into data registers and address registers.
- **Data Registers** are used to hold numeric values such as integer and floating-point values. In some older and low end CPUs, a special data register, known as the **accumulator**, is used implicitly for many operations.
- Address Registers hold addresses and are used by instructions that indirectly access memory.
- **Conditional Registers** hold truth values often used to determine whether some instruction should or should not be executed.
- General Purpose Registers (GPRs) can store both data and addresses, i.e., they are combined Data/Address registers.
- Floating Point Registers (FPRs) store floating point numbers in many architectures.
- Constant Registers hold read-only values such as zero, one, or pi.
- Vector Registers hold data for vector processing done by SIMD instructions (Single Instruction, Multiple Data).
- Special Purpose Registers (SPR) hold program state; they usually include the program counter (or instruction pointer), stack pointer, and status register (or processor status word).
- In some architecture, **Model-Specific Registers** (also called *machine-specific registers*) store data and settings related to the processor itself. Because their meanings are attached to the design of a specific processor, they cannot be expected to remain standard between processor generations.
- Registers related to fetching information from RAM, a collection of storage registers located on separate chips from the CPU (unlike most of the above, these are generally not *architectural* registers):These registers are:-

- Memory Address Register (MAR):- Connected to the address lines of the system bus. It specifies the address of memory location from which data or instruction is to be accessed (for read operation) or to which the data is to be stored (for write operation).
- Memory Buffer Register (MBR):- Connected to the data lines of the system bus. It specifies which data is to be accessed (for read operation) or to which data is to be stored (for write operation).
- Memory Data Register (MDR): is the register that contains the data to be stored in the computer storage (e.g. RAM), or the data after a fetch from the computer storage. It acts like a buffer and holds anything that is copied from the memory ready for the processor to use it.
- Memory Type Range Registers (MTRR): Registers in the Pentium Pro and Pentium II processors that can be used to specify a strategy for communication with the external memory and caches for a number of physical address ranges.
- Hardware registers are similar, but occur outside CPUs.
- **Program Status Word (PSW):-** Condition registers, or flags, are used to maintain status information. Some architectures contain a special program status word (PSW) register. The PSW contains bits that are set by the CPU to indicate the current status of an executing program. These indicators are typically for arithmetic operations, interrupts, memory protection information, or processor status.
- Control and Status Registers It has three types:

Program Counter (PC):- Holds address of next instruction to be fetched, after the Execution of an on-going Instruction.

Instruction Register (IR):- Here the instruction are loaded before their execution

Index Register: In index addressing, the address of the operand is obtained by adding a constant to the content of a register, called the index register. The index register holds an address displacement.

Segment Pointers: In order to support segmentation, the address issued by the processor should consist of a segment number (base) and a displacement (or an offset) within the segment. A segment register holds the address of the base of the segment.

Stack Pointer: A stack is a data organization mechanism in which the last data item stored is the first data item retrieved. Two specific operations can be performed on a stack. These are the **Push and the Pop operations**. A specific register, called the **Stack Pointer (SP)**, is used to indicate the stack location that can be addressed. In the stack **PUSH** operation, the SP value is used to indicate the location (called the top of the stack). After storing (pushing) this value, the SP is **incremented** In the stack push operation, the SP value is used to indicate the location (called the top of the stack) in which the value is to be stored (in our example it is location 1023). After storing (pushing) this value the SP isincremented to indicate to location 1024.



Fig. 7.4: Push & Pop Operations

In the stack **pop** operation, the SP is first **decremented** to become 1021. The value stored at this location (DD in our example) is retrieved (popped out) and stored in the shown register grows low in memory).

Stack Machine: 'Stack machine' commonly refers to computers which use a Last-in, First-out stack to hold short-lived temporary values while executing individual program statements. The instruction set carries out most ALU actions with postfix (Reverse Polish notation) operations that work only on the expression stack, not on data registers or main memory cells.

Block diagram of Stack Machine

A block diagram of Stack Machine's consists components like:

- Data Bus,
- Data Stack (DS),
- Return Stack (RS),
- Arithmetic/Logic Unit (ALU)
- Top of Stack Register (TOS),
- Program Counter (PC),
- program memory with a Memory Address Register (MAR),
- control logic with an Instruction Register (IR), and
- Input/Output section (I/O).



Fig. 7.5 Block Diagram of Stack Machine

Accumulator: is a register in which intermediate arithmetic and logic results are stored. Without a register like an accumulator, it would be necessary to write the result of each calculation (addition, multiplication, shift, etc.) to main memory and to be read right back again for use in the next operation. We know that access to main memory is slower than access to a register like the accumulator because the technology used for the large main memory is slower (but cheaper) than that used for a register. This is a model of a generic zero-address computer.

The canonical example for accumulator use is summing a list of numbers. The accumulator is initially set to zero, then each number in turn is added to the value in the accumulator. Only when all numbers have been added is the result held in the accumulator written to main memory or to another, non-accumulator, CPU register.

An accumulator machine, also called a 1-operand Machine, or a CPU with accumulator-based architecture, is a kind of CPU in which—although it may have several registers—the CPU always stores the results of most calculations in one special register—typically called "the" accumulator of that CPU. Historically almost all early computers were accumulator machines; and many microcontrollers still popular as of 2010 (such as the 68HC12, the PICmicro, the 8051 and several others) are basically accumulator machines.

An accumulator-based processor, which has **Five 16-bit registers:** Program Counter (PC), Instruction Register (IR), Address Register(AR), Accumulator (AC), and Data Register (DR) as shown in fig. 7.6



Fig. 7.6: Accumulator based Machine

80X86 Registers

The architecture of 80X86 Processor consists of Three register groups. These are

- · General-purpose Registers,
- · Segment Registers, and the Instruction Pointer (Program Counter) and
- Flag Register.

The first set consists of general purpose registers A, B, C, D, SI (source index), DI (Destination Index), SP (Stack Pointer), and BP (Base Pointer).

The second set of registers consists of CS (Code Segment), SS (Stack Segment), and four data segment registers DS, ES, FS, and GS.

The third set of registers consists of the instruction pointer (program counter) and the flags (status) register.

7.3.2 Arithmetic Unit

The Arithmetic Logic Unit (ALU) and the Control Unit (CU) together are termed as the Central Processing Unit (CPU). The CPU is the most important component of a computer's hardware. The ALU performs the arithmetic operations such as addition, subtraction, multiplication and division, and the logical operations such as: "Is A =B?" (Where A and B are both numeric and alphanumeric data), "Is a given character equal to M (for male) or F (for female)?" The control unit interprets instructions and produces the respective control signals. All the arithmetic and logical Operations are performed in the CPU in special storage areas called Registers.

7.3.3 CONTROL UNIT

The control unit is the main component that directs the system operations by sending control signals to the datapath. These signals control the flow of data within the CPU and between the CPU and external units such as memory and I/O. Control buses generally carry signals between the control unit and other computer components in a clock-driven manner. The system clock produces a continuous sequence of pulses in a specified duration and frequency. A sequence of steps t0, t1, t2, ..., are used to execute a certain instruction.

The op-code field of a fetched instruction is decoded to provide the control signal generator with information about the instruction to be executed. Step information generated by a logic circuit module is used with other inputs to generate control signals. The signal generator can be specified simply by a set of Boolean equations for its output in terms of its inputs. Figure 7.7 shows a block diagram that describes how timing is used in generating control signals.



Fig. 7.7: Timing of control signals

To execute instructions, a processor must generate the control signals used to perform the processor's actions in the proper sequence. This sequence of actions can either be executed by another processor's software or in hardware.

The signals generating methods fall into two categories:

(i) Hardwired control, in which the instruction bits directly generate the signals. In hardwired control, fixed logic circuits that correspond directly to the Boolean expressions are used to generate the control signals.

(ii) Microprogrammed Control in which a dedicated microcontroller executes a microprogram to generate the signals.

In microprogrammed control, the control signals associated with operations are stored in special memory units inaccessible by the programmer as control words. A **control word** is a microinstruction that specifies one or more microoperations. A sequence of microinstructions is called a **microprogram**, which is stored in a ROM or RAM called a **Control Memory (CM)**.

Hard wired vs Micro-programmed Control

Hardwired control is faster than microprogrammed control. However, hardwired control could be very expensive and complicated for complex systems. Hardwired control is more economical for **small control units.** It should also be noted that micro programmed control could adapt easily to changes in the system design. We can easily add new instructions without changing hardware. Hardwired control will require a Re-design of the entire systems in the case of any change.

Hard-Wired Control Implementation

- It is implemented as logic circuits (gates, flip-flops, decoders etc.) in the hardware.
- This organization is very complicated if we have a large control unit.
- In this organization, if the design has to be modified or changed, requires changes in the wiring among the various components. Thus the modification of all the combinational circuits may be very difficult

Hard wired Control organization's architecture consists of consist of :

- Instruction Register
- Number of Control Logic Gates,
- · Two Decoders
- 4-bit Sequence Counter



Fig. 7.8: Architecture of Hard-wired Organization

How it is Works

An instruction read from memory is placed in the Instruction Register (IR).

The instruction register is divided into three parts:

• bit,

· operation code, and

• address part.

First 12-bits (0-11) to specify an address, next 3-bits specify the operation code (opcode) field of the instruction and last left most bit specify the addressing mode I.

I = 0 for direct address

I = 1 for indirect address

First 12-bits (0-11) are applied to the control logic gates.

The operation code bits (12 - 14) are decoded with a 3 x 8 decoder.

The eight outputs (D0 through D7) from a decoder goes to the control logic gates to perform specific operation.

Last bit 15 is transferred to a I flip-flop designated by symbol I.

The 4-bit Sequence Counter (SC) can count in binary from 0 through 15.

The counter output is decoded into 16 timing pulses T0 through T15.

The sequence counter can be incremented by INR input or clear by CLR input synchronously.

Example

Consider the case where SC is incremented to provide timing signalsT0, T1, T 2, T3, and T4 in sequence. At time T4, SC is cleared to 0 if decoder output D3 is active. This is expressed symbolically by the statement:

D3 T4 : SC

The timing diagram shows the time relationship of the control signals



Fig. 7.9: Timing Diagram

Microprogrammed control Organization

Microprogrammed control is a control mechanism to generate control signals by using a memory called **Control Storage (CS)**, which contains the control signals.

Maurice Wilkes invented "**microprogram**" in 1953. He realised an idea that made a control unit easier to design and is more flexible. His idea is that a control unit can be implemented as a memory which contains patterns of the control bits and part of the flow control for sequencing those patterns. Microprogram control organization works to control sequence patterns of control bits. Using microprogram, a control organization can be implemented for a complex instruction set which is impossible to do by hardwired.

Some Important Terms

- **Micro-Instructions**: The instructions that make micro-program are called micro-instructions. A micro-instruction consists of:
 - One or more micro-operations to be executed.
 - Address of next microinstruction to be executed.
- Micro-Operations: The operations performed on the data stored inside the registers are called micro-operations.
- **Micro-Programs:** Microprogramming is the concept for generating control signals using programs. These programs are called micro-programs.
- Micro-Code: Micro-program is a group of microinstructions. The micro-program can also be termed as micro-code.
- **Control Memory:** Micro-programs are stored in the read only memory (ROM). That memory is called control memory

Microprogrammed control seems to be advantageous to CISC machines, since CISC requires systematic development of sophisticated control signals, there is no intrinsic difference between these 2 control mechanism.

Microprogrammed control unit composed of microprogram PC, micro memory, output buffer and a sequencing unit.

Micro Memory (sometime called micro store) contains bit patterns that are used to control the datapath. Each word of micro memory is separated into several fields: internal control, external control, conditional, next address.

- 1. Internal control bits are the signals that control the datapath.
- 2. External control bits are the signals that control external unit such as memory (read, write), interrupt acknowledge etc.
- Conditionals are the bits that are used to determine the flow of microprogram; loop, branching, next instruction etc. Its input comes from the datapath (usually from the conditional code register). Next address determines the next microword to be executed.

A microprogram is executed as follow :

1. A word from microprogram at the location specified by the microPC is read out, control bits are latched at the output buffer which is connected to the datapath.

2. If conditional field is specified and the test for conditional is true, the next address of microprogram will come from the next address field otherwise the microPC will be incremented (execute the next microword).



Fig. 7.10: Micro controlled Organization

Figure 7.10 shows the general configuration of a **microprogrammed control.** The **Control Memory** is assumed to be a ROM within which all control information is permanently stored. The Control Address Register (CAR) specifies the address of the microinstruction. The Control Data Register (CDR), which is optional, may hold the microinstruction currently being executed by the datapath and the control unit.

One of the functions of the control word is to determine the address of the next microinstruction to be executed. This microinstruction may be the next one in sequence, or it may be located somewhere else in the control memory. Therefore, one or more bits that specify how to determine the address of the next microinstruction must be present in the current microinstruction.

The next address may also be a function of status and external control inputs. While a microinstruction is being executed, the next-address generator produces the next address. This address is transferred to the CAR on the next clock pulse and is used to read the next microinstruction to be executed from

ROM. Thus, the microinstructions contain bits for activating microoperations in the datapath and bits that specify the sequence of microinstructions executed. The next-address generator, in combination with the CAR, is sometimes called a microprogram sequencer, as it determines the sequence of instructions that is read from control memory.

The address of the next microinstruction can be specified in several ways, depending on the sequencer inputs. Typical functions of a microprogram sequencer are incrementing the CAR by one and loading the CAR. Possible sources for the load operation include an address from control memory, an externally provided address, and an initial address to start control unit operation. The CDR holds the present microinstruction while the next address is being computed and the next microinstruction is being read from memory. The CDR breaks up a long combinational delay path through the control memory and the datapath. Insertion of this register is just like inserting a pipeline platform, it allows the system to use a higher clock frequency and hence perform processing faster.

The inclusion of a CDR in a system, however, complicates the sequencing of microinstructions, particularly when decision making based on status bits is involved. Hence, for simplicity, we omit the CDR and take the microinstructions directly from the ROM outputs. The ROM operates as a combinational circuit, with the address as the input and the corresponding microinstruction as the output.

The contents of the specified word in ROM remain on the output lines of the ROM as long as the address value is applied to the inputs. No read/write signal is needed, as it is with RAM. Each clock pulse executes the microoperations specified by the microinstruction and also transfers a new address to the CAR, which, in this case, is the only component in the control that receives clock pulses and stores state information. The next-address generator and the control memory are combinational circuits. Thus, the state of the control unit is given by the contents of the CAR. The status bits enter the next-address generator and affect the determination of the next state. Unless the status bits bypass the control unit and directly control the microoperations being executed in the datapath, they can do no more than select the next microoperation by affecting the address generated by the nextaddress generator.

Micro-program Word Length

Based on 3 factors

- · Maximum number of simultaneous micro-operations supported
- · The way control information is represented orencoded
- · The way in which the next micro-instruction address is specified

Micro-instruction Types

- Each micro-instruction specifies single (or few) micro-operations to be performed (vertical microprogramming)
- Each micro-instruction specifies many different micro-operations to be performed in parallel(horizontal micro-programming)

Horizontal microprogram allows each control bit to be independent from other therefore enables maximum simultaneous events and also offers great flexibility. It is also waste a lot bit. For each field of microword, there may be a group of bits that are not activated at the same time therefore they can be

"encoded" to use a fewer bit. A decoder is required to "decode" these bits and to connect them to the datapath. This approach is called **vertical microprogram.**

Vertical Micro-programming

- Width is narrow
- n control signals encoded into log2 n bits
- · Limited ability to express parallelism
- Considerable encoding of control information requires external memory word decoder to identify the exact control line being manipulated



Fig. 7.11: Vertical Micro Programming

Horizontal Micro-programming

- Wide memory word
- High degree of parallel operations possible
- Little encoding of control information



Fig. 7.12 Horizontal Micro-Programming

Microprogram becomes obsolete mainly because the present design emphasises the performance and microprogram is slower than hardwired. The change in instruction set design toward a minimum number of clock per instruction simplifies the instruction set to the point that microprogram is not really required. Also the design of hardwired control unit can be mostly automated as opposed to microprogram which must be "written" and "debug". Hence, for the current instruction set architecture, hardwired control unit offers a lower engineering cost.

Advantages

- The design of micro-program control unit is less complex becausemicro-programs are implemented using software routines.
- The micro-programmed control unit is more flexible because designmodifications, correction and enhancement is easily possible.
- The new or modified instruction set of CPU can be easily implemented by simply rewriting or modifying the contents of control memory.
- The fault can be easily diagnosed in the micro-program control unitusing diagnostics tools by maintaining the contents of flags, registers and counters.

Disadvantages

- The micro-program control unit is slower than hardwired control unit. That means to execute an instruction in micro-program control unitrequires more time.
- The micro-program control unit is expensive than hardwired controlunit in case of limited hardware resources.
- The design duration of micro-program control unit is more thanhardwired control unit for smaller CPU.

CPU Organization–Summary

- **1.(a)** A CPU can be defined as a general purpose instruction set processor responsible for program execution.
 - (b) A CPU consists of address bus, data bus and control bus.
 - (c) A computer with one CPU is called microprocessor and with more than one CPU in called multiprocessor.
 - (d) The address bus in used to transfer addresses from the CPU to main memory or to I/O devices
 - (e) Data bus is the main path by which information is transferred to and from the CPU
 - (f) Control bus is used by CPU to control various devices connected and to synchronise their operations with those of the CPU.
- 2. (a) A control unit take the instructions one by one to execute. It takes data from input devices and store it in memory. And also sends data from memory to the output device.
 - (b) All arithmetic and logical operations are carried out by Arithmetic Logical Unit
 - (c) A control unit and the arithmetic logical unit together is known as CPU
 - (d) can be : Hardwired & Microprogrammed
- 3.(a) The accumulator is the main register of the ALU
 - (b) In execution of the most of the instructions the accumulator is used to store a input data or output result.
 - (c) Instructions register holds the opcode of the current instruction
 - (d) Memory address register holds the address of the current instructions.
- 4. A accumulator based CPU consists of (a) data processing unit (b) program control unit and (c) memory and I/O interface unit.

- (a) (i) In the data processing unit, data is processed to get some results.
 - (ii) the accumulator in the main operand register of the ALU.
- (b) (i) Program control unit controls various parts of CPU.
 - (ii) Program counter holds the address of the next instructions to be read from memory after the current instruction is executed.
 - (iii) Instruction register holds the opcode of the current instruction.
 - (iv) Control circuits hold the responsibility of every operation of the CPU.
- (c) (i) Data registers of the memory and I/O interface unit acts as a buffer between the CPU and main memory.
 - (ii) Address register contains the address of the present instructions obtained from the program control unit.
- **5.(a)** Stack pointer and flag register are special registers of CPU.
 - (b) Stack pointers holds the address of the most recently entered item into the stack.
 - (c) Flag registers indicates the status which depends on the results of the operation.
- 6.(a) Micro operations are the operations executed on data stored in registers.
 - (b) A set of micro operations specified by an instruction is known as macro operation.
- 7.(a) A sequence of operations involved in processing an instruction constitutes an instruction cycle
 - (b) Fetch cycle in defined as the time required for getting the instruction code from main memory to CPU
 - (c) Executed cycle is the time required to decode and execute an instruction.
 - (d) Fetch cycle requires a fixed time slot and execute cycle requires variable time slot.
- 8.(a) a word length indicates the number of bits the CPU can process at a time.
 - (b) A memory size indicates the total storage capacity of the CPU.
 - (c) Word length is the indication of bit length of each register.
- **9.** A computer is said to be operated based on stored program concept if it stores the instructions as well as data of a program in main memory when they are waiting to execute.
- **10.** A stored program in main memory is executed instruction after instruction in a successive method by using program counter.

7.4 CPU DATAPATH

The CPU can be divided into a **Data Section and a Control Section**. The data section, which is also called the **Datapath**, contains the registers and the ALU. The datapath is capable of performing certain operations on data items. The control section is basic all the control unit, which issues control signals to the datapath. Internal to the CPU, data move from one register to another and between ALU and registers.

Internal data movements are performed via local buses, which may carry data, instructions, and addresses

Simple architecture of datapath consists of components like memory (stores the current instruction), *PC* or Program Counter (stores the address of current instruction), and *ALU* (executes current instruction). The interconnection of these simple components to form a basic datapath is illustrated in Fig. 7.12.



Fig. 7.13: Interconnection of various components in DataPath

In computer organization Data move from registers to memory and I/O devices, often by means of a system bus. Internal data movement among registers and between the ALU and registers may be carried out using different organizations including **one-bus**, **two-bus**, **or three-bus organizations**. Dedicated datapaths may also be used between components that transfer data between themselves more frequently. For example, the contents of the PC are transferred to theMAR to fetch a new instruction at the beginning of each instruction cycle. Hence, a dedicated datapath from the PC to the MAR could be useful in speeding up this part of instruction execution.

7.4.1 One-bus Organization

Using one bus, the CPU registers and the ALU use a single bus to move outgoing and incoming data. Since a bus can handle only a single data movement within one clock cycle, two-operand operations will need two cycles to fetch the operands for the ALU. Additional registers may also be needed to buffer data for the ALU.

This bus organization is the simplest and least expensive, but it limits the amount of data transfer that can be done in the same clock cycle, which will slow down the overall performance. Figure 7.14 shows a one-bus datapath consisting of a set of general-purpose registers, a memory address register (MAR), a memory data register (MDR), an instruction register (IR), a program counter (PC), and an ALU.



Fig. 7.14: one bus data Path
7.4.2: Two Bus Organization

Using two buses is a faster solution than the one-bus organization. In this case, general-purpose registers are connected to both buses. Data can be transferred from twodifferent registers to the input point of the ALU at the same time. Therefore, a twooperandoperation can fetch both operands in the same clock cycle.



Fig. 7.15: Two-Bus Organization

An additional buffer register may be needed to hold the output of the ALU when the two buses are busy carrying the two operands. In some cases, one of the buses may be dedicated for moving data into registers (in-bus), while the other is dedicated for transferring data out of the registers (out-bus). In this case, the additional buffer register may be used, as one of the ALU inputs, to hold one of the operands. The ALU output can be connected directly to the in-bus, which will transfer the result into one of the registers. Figure 7.15 shows a two-bus organization with in-bus and out-bus.

7.4.3. Three-Bus Organization

In a three-bus organization, two buses may be used as source buses while the third is used as destination. The source buses move data out of registers (out-bus), and the destination bus may move data into a register (in-bus). Each of the two out-buses is connected to an ALU input point. The output of the ALU is connected directly to the in-bus. As can be expected, the more buses we have, the more data we can move within a single clock cycle. However, increasing the number of buses will also increase the complexity of the hardware.



Fig. 7.16: shows an example of a three-bus datapath

7.4.4 Single Cycle Datapath Vs Multicycle Datapath

A single-cycle datapath executes in one cycle all instructions. This clearly impacts CPI in a beneficial way, namely, CPI = 1 cycle for all instructions. we use the single-cycle datapath components to create a multi-cycle datapath, where each step in the fetch-decode-execute sequence takes one cycle. This approach has **Two** advantages over the single-cycle datapath:

- 1. Each functional unit (e.g., Register File, Data Memory, ALU) can be used more than once in the course of executing an instruction, which saves hardware (and, thus, reduces cost); and
- 2. Each instruction step takes one cycle, so different instructions have different execution times. In contrast, the single-cycle datapath that we designed previously required every instruction to take one cycle, so all the instructions move at the speed of the slowest.

7.5 GLOSSARY

Pipe-lined Architecture:- In pipelined architecture of computers many instructions executed in singe cycle to increase their instruction throughput

Non-Pipelined Architecture : In this architecture of CPU instructions are executed serially, and CPU doesn't supply clock to entire circuit

User-accessible Registers - The most common division of user-accessible registers is into data registers and address registers.

Data Registers are used to hold numeric values such as integer and floating-point values.

Address Registers hold addresses and are used by instructions that indirectly access memory.

Conditional Registers hold truth values often used to determine whether some instruction should or should not be executed.

General Purpose Registers (GPRs) can store both data and addresses, i.e., they are combined Data/Address registers.

Floating Point Registers (FPRs) store floating point numbers in many architectures.

Constant Registers hold read-only values such as zero, one, or pi.

Vector Registers hold data for vector processing done by SIMD instructions (Single Instruction, Multiple Data).

Special Purpose Registers (SPR) hold program state; they usually include the program counter, stack pointer, and status register

Instruction Registers store the instruction currently being executed

Memory Address Register (MAR):- Connected to the address lines of the system bus.

Memory Buffer Register (MBR):- Connected to the data lines of the system bus. It specifies which data is to be accessed (for read operation) or to which data is to be stored (for write operation).

Memory Data Register(MDR): is the register that contains the data to be stored in the computer storage (e.g. RAM), or the data after a fetch from the computer storage.

Memory Type Range Registers (MTRR): can be used to specify a strategy for communication with the external memory and caches for a number of physical address ranges.

Memory Type Range Registers (MTRR): Registers in the Pentium Pro and Pentium II processors that can be used to specify a strategy for communication with the external memory and caches for a number of physical address ranges.

Hardware Registers are similar, but occur outside CPUs.

Program Status Word (PSW).:-. The PSW contains bits that are set by the CPU to indicate the current status of an executing program.

Program Counter (PC):- Holds address of next instruction to be fetched, after the Execution of an on-going Instruction.

Instruction Register (IR):- Here the instruction are loaded before their execution

Index Register:. The index register holds an address displacement.

Segment Pointers: A segment register holds the address of the base of the segment.

Stack Pointer: A stack pointer holds the address of stack

Stack Machine: commonly refers to computers which use a Last-in, First-out stack to hold short-lived temporary values while executing individual program statements.

Accumulator is a register in which intermediate arithmetic and logic results are stored.

Arithmetic Unit :performs the arithmetic operations such as addition, subtraction, multiplication and division, and the logical operations

Control Unit: is the main component that directs the system operations by sending control signals to the datapath

Hardwired control, in which the instruction bits directly generate the signals.

Microprogrammed control in which a dedicated microcontroller executes a micro program to generate the signals.

Micro-Instructions: The instructions that make micro-program are called micro-instructions.

Micro-Operations: The operations performed on the data stored inside the registers .

Micro-Programs: Microprogramming is the concept for generating control signals using programs.

Micro-Code: Micro-program is a group of microinstructions. The micro-program can also be termed as micro-code.

Control Memory: Micro-programs are stored in the read only memory (ROM). That memory is called control memory.

Datapath: The data section, which is also called the datapath, contains the registers and the ALU.

7.6 REVIEW QUESTIONS

Q.1 How pipe-lining enhance the performance of CPU and How it is works?

Q.2 What are the basic differences between Non-pipes lined and pipelined architecture of CPU.

Q.3 Define the following types of Registers(i) GPR(ii) SPR(iii) MAR(iv)MDR(v)MTRR(vi)PC

Q.4 Describes the Stack Machine and Accumulator machines.

Q.5 Write the Hard-wired and Micro-programmed control organization with detailed architecture.

Q.6 Differentiate between :

- (i) Hard-wired & Micro-programmed
- (ii) Horizontal & vertical Micro-programming
- (iii) MDR and MBR
- (iv) Micro-Program, Micro-Instruction & Micro-operation
- (v) Single vs. Multi cycle Datapath
- Q.7 During which stage of the instruction execution cycle is the program counter incremented?
- **Q.8** Define pipelined execution.
- **Q.9** In a 5-stage non-pipelined processor, how many clock cycles would it takes to execute 2 instructions?
- Q.10 What do you mean by DataPath? Discuss various organizations of Datapath.

Chapter 8

Addressing Mode, Instruction Format, Type and I/O Techniques

8.0 OBJECTIVES

After going through this chapter you should able to understand the concepts of:

- Concept of Addressing Modes: ZERO, ONE, ONE & HALF, TWOTHREE
- · Modes: Immediate, Direct, In-Direct, Indexed, Auto Increment,
- Instruction Format
- Instruction Cycle: Fetch, Decode, Execute, Reload

8.1 ADDRESSING MODES

Information involved in any operation performed by the CPU needs to be addressed. In computer terminology, such information is called the **operand.** Therefore, any instruction issued by the processor must carry at least two types of information.

These are the operation to be performed, encoded in what is called the **op-code** field, and the address information of the operand on which the operation is to be performed, encoded in what is called the **address field**.

Instructions can be classified based on the number of operands as:

- (a) Three-address,
- (b) Two-address,
- (c) One-and-half-address,
- (d) One-address, and
- (e) Zero-address.

We explain these classes together with simple examples in the following paragraphs:

A three-address instruction takes the form operation add-1, add-2, add-3. In this form, each of add-1, add-2, and add-3 refers to a register or to a memory location. Consider, for example, the instruction ADD R1, R2, R3.

An example of a three-address instruction that refers to memory locations may take the form ADD A,B,C. The instruction adds the contents of memory location A to the contents of memory location B and stores the result in memory location C.

A Two-address Instruction takes the form operation add-1, add-2. In this form, each of add-1 and add-2 refers to a register or to a memory location. Consider, for example, the instruction ADD R1, R2. This instruction adds the contents of register

R1 to the contents of register R2 and stores the results in register R2. The original contents of register R2 are lost due to this operation while the original contents of register R1 remain intact. This instruction is equivalent to a three-address instruction of the form ADD R1,R2,R2. A similar instruction that uses memory locations instead of registers can take the form ADD A,B. In this case, the contents of memory location A are added to the contents of memory location B and the result is used to override the original contents of memory location B.

The operation performed by the three-address instruction ADD A,B,C can be performed by the two two-address instructions MOVE B,C and ADD A,C. This is because the first instruction moves the contents of location B into location C and the second instruction adds the contents of location A to those of location C (the contents of location B) and stores the result in location C.

A One-address Instruction takes the form ADD R1. In this case the instruction implicitly refers to a register, called the Accumulator R_{acc} , such that the contents of the accumulator is added to the contents of the register R1 and the results are stored back into the accumulator R_{acc} . If a memory location is used instead of a register then an instruction of the form ADD B is used. In this case, the instruction adds the content of the accumulator Racc to the content of memory location B and stores the result back into the accumulator Racc. The instruction ADD R1 is equivalent to the three-address instruction ADD R1, R_{acc} , R_{acc} or to the two-address instruction ADD R1, R_{acc} .

Between the two- and the one-address instruction, there can be a **One-and-Half Address Instruction.** Consider, for example, the instruction ADD B, R1. In this case, the instruction adds the contents of register R1 to the contents of memory location B and stores the result in register R1. Owing to the fact that the instruction uses two types of addressing, that is, a register and a memory location, it is called a one-and-half-address instruction. This is because register addressing needs a smaller number of bits than those needed by memory addressing.

It is interesting to indicate that there exist **Zero-address Instructions**. These are the instructions that use stack operation. A stack is a data organization mechanism in which the last data item stored is the first data item retrieved. Two specific operations can be performed on a stack. These are the push and the pop operations.

Instruction Class	Example
Three-address	ADD R_1, R_2, R_3
	ADD A,B,C
Two-address	ADD R_1, R_2
	ADD A, B
One-and-half-address	ADD B, R_1
One-address	Add R_1
Zero-address	ADD (<i>SP</i>) +, (<i>SP</i>)

Fig. 8.1:	Varioustypes of	' Add	dressing I	Modes
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The different ways in which operands can be addressed are called the **addressing modes**. Addressing modes differ in the way the address information of operands is specified. The simplest addressing mode is to include the operand itself in the instruction, that is, no address information is needed. This is called **immediate addressing**. A more involved addressing mode is to compute the address of the operand by adding a constant value to the content of a register. This is called **indexed addressing**. Between these two addressing modes there exist a number of other addressing modes including **absolute addressing**, **direct addressing**. A number of different addressing modes are explained below.

8.1.1 Immediate Mode

According to this addressing mode, the value of the operand is (immediately) available in the **instruction itself**. Consider, for example, the case of loading the decimal value 1000 into a register R_i . This operation can be performed using an instruction such as the following: LOAD #1000, R_i . In this instruction, the operation to be performed is to load a value into a register. The source operand is (immediately) given as 1000, and the destination is the register R_i .

It should be noted that in order to indicate that the value 1000 mentioned in the instruction is the operand itself and not its address (immediate mode), it is customary to prefix the operand by the special character (#). As can be seen the use of the immediate addressing mode is simple.

The use of immediate addressing leads to poor programming practice. This is because a change in the value of an operand requires a change in every instruction that uses the immediate value of such an operand. A more flexible addressing mode is explained below.

8.1.2 Direct (Absolute) Mode

According to this addressing mode, the address of the memory location that holds the operand is **included in the instruction**. Consider, for example, the case of loading the value of the operand stored in memory location 1000 into register R_i . This operation can be performed using an instruction such as LOAD 1000, Ri. In this instruction, the source operand is the value stored in the memory location whose address is 1000, and the destination is the register R_i . Note that the value 1000 is not prefixed with any special characters, indicating that it **is the (direct or absolute) address of the source operand**.

Figure 8.2 shows an illustration of the direct addressing mode. For example, if the content of the memory location whose address is 1000 was (2345) at the time when the instruction LOAD 1000, Ri is executed, then the result of executing such instruction is to load the value (2345) into register Ri. Direct (absolute) addressing mode provides more flexibility compared to the immediate mode. However, it requires the explicit inclusion of the operand address in the instruction. A more flexible addressing mechanism is provided through the use of the indirect addressing mode. This is explained below.



Fig.8.2: Illustration of Direct Addressing Mode

8.1.3 Indirect Mode

In the indirect mode, what is included in the instruction is not the address of the operand, but rather a name of a register or a memory location that holds the (effective) address of the operand. In order to indicate the use of indirection in the instruction, it is customary to include the name of the register or the memory location in parentheses. Consider, for example, the instruction LOAD (1000), R_i . This instruction has the memory location 1000 enclosed in parentheses, thus indicating indirection.

The meaning of this instruction is to load register R_i with the contents of the memory location whose address is stored at memory address 1000. Because indirection can be made through either a register or a memory location, therefore, we can identify two types of indirect addressing. These are register indirect addressing, if a register is used to hold the address of the operand, and memory indirect addressing, if a memory location is used to hold the address of the operand. The two types are illustrated in Figure 8.3



Fig.8.3 Illustration of In-Direct Addressing Mode

8.1.4 Indexed Mode

In this addressing mode, the address of the operand is obtained by adding a constant to the content of a register, called the index register. Consider, for example, the instruction LOAD X(Rind), Ri. This instruction loads register Ri with the contents of the memory location whose address is the sum of the contents of register Rind and the value X. Index addressing is indicated in the instruction by including the name of the index register in parentheses and using the symbol X to indicate the constant to be added. Figure 8.4 illustrates indexed addressing. As can be seen, indexing requires an additional level of complexity over register indirect addressing.



Fig.8.4: Illustration of Indexed Addressing Mode

8.1.5 Other Modes

The addressing modes presented above represent the most commonly used modes in most processors. They provide the programmer with sufficient means to handle most general programming tasks. However, a number of other addressing modes have been used in a number of processors to facilitate execution of specific programming tasks. These additional addressing modes are more involved as compared to those presented above. Among these addressing modes the **relative**, **autoincrement**, **and the autodecrement** modes represent the most well-known ones. These are explained below.

8.1.5.1 Relative Mode

Recall that in indexed addressing, an index register, Rind, is used.

Relative addressing is the same as indexed addressing except that the Program Counter (PC) replaces the index register. For example, the instruction LOAD X(PC), Ri loads register Ri with the contents of the memory location whose address is the sum of the contents of the program counter (PC) and the value X. Figure 8.5 illustrates the relative addressing mode.



Fig.8.5 Relative Addressing Mode

8.1.5.2 Autoincrement Mode

This addressing mode is similar to the register indirect addressing mode in the sense that the effective address of the operand is the content of a register, call it the autoincrement register, that is included in the instruction, However, with autoincrement, the content of the autoincrement register is automatically incremented after accessing the operand.

8.1.5.3 Autodecrement

Mode Similar to the autoincrement, the autodecrement mode uses a register to hold the address of the operand. However, in this case the content of the autodecrement register is first decremented and the new content is used as the effective address of the operand.

Address mode	Example	Meaning	When used	
Register	Add R4, R3	Regs (R4) = Regs (R4) + Regs (R3)	When a value is in a register	
Immediate Register indirect	Add R4 R3 Add R4 (1001)	Regs (R4) = Regs (R4) +3	For Constants	
Direct or absolute	ADD R4 (1001)	Regs(R4) = Regs (R4) + Mem (1001))	Accessing using a pointer or a computed address	
Displacements	Add R4, (00(R1)	Rogs (R4) - Regs (R4) + Mem (100 + Regs (R1))	Sometimes useful for accessing static data, address constant may need to be large	
indexed	Add R4, (00(R1-R2)	Regs (R4) = Regs (R4) + Mem (100 +Hegs(R1))	Accossing local variables	
Auto increment	Add R4, (R2)	Regs(R4) = Regs (R4) + Mem(Regs(R2) - d Regs(R2) = Regs (R2) + d	Useful for slepping through arrays within a loop R2 point to start of the array each reference increaments R2 by d	
Auto Decrement	Add R4, (R2)	Regs (R2) = Regs(R2) – d Regs (R4) = Regs(R4) Mem(Regs(R2)	Same use as auto-incremant Autodecrement/increment can implement a stack	
Scaled	Add R4, 100 (R2) (R3)	Regs (R4) = Regs(R4) + Mem(100 + Hegs (R2) + Degs(R3) + d1	Used to index arrays	

Table 8.0: Summary of Various Address Mode

8.2 INSTRUCTION FORMATS

- It is the function of the control unit within the CPU to interpret each instruction code
- The bits of the instruction are divided into groups called fields
- The most common fields are:
 - Operation code
 - Address field memory address or a processor register
 - Mode field specifies the way the operand or effective address is determined
- A register address is a binary number of k bits that defines one of 2k registers in the CPU
- The instructions may have several different lengths containing varying number of addresses
- The number of address fields in the instruction format of a computer depends on the internal organization of its registers
- Most computers fall into one of the three following organizations:
 Single accumulator organizationo General register organizationo Stack organization
- Single accumulator org. uses one address field ADD X : AC \leftarrow AC + M[X]
- The general register org. uses three address fields ADD R1, R2, R3: R1 ← R2 + R3
- Can use two rather than three fields if the destination is assumed to be one of the source registers
- Stack org. would require one address field for PUSH/POP operations and none for operation-type instructions

PUSH X

ADD

· Some computers combine features from more than one organizational structure

Example:

X = (A+B) * (C + D)

Three-address instructions:

ADD R1, A, B R1 \leftarrow M[A] + M[B] ADD R2, C, D R2 \leftarrow M[C] + M[D] MUL X, R1, R2 M[X] \leftarrow R1 * R2

Two-address instructions:

MOV R1, A R1 \leftarrow M[A] ADD R1, B R1 \leftarrow R1 + M[B] MOV R2, C R2 \leftarrow M[C] ADD R2, D R2 \leftarrow R2 + D MUL R1, R2 R1 \leftarrow R1 * R2 MOV X, R1 M[X] \leftarrow R1

One-address instructions

LOAD A AC \leftarrow M[A] ADD B AC \leftarrow AC + M[B] STORE T M[T] \leftarrow AC LOAD C AC \leftarrow M[C] ADD D AC \leftarrow AC + M[D] MUL T AC \leftarrow AC * M[T] STORE X M[X] \leftarrow AC

Zero-address instructions

PUSH A TOS \leftarrow A PUSH B TOS \leftarrow B ADD TOS \leftarrow (A +B) PUSH C TOS \leftarrow C PUSH D TOS \leftarrow D ADD TOS \leftarrow (C + D) MUL TOS \leftarrow (C + D) * (A + B) POP X M[X] \leftarrow TOS

RISC instructions

LOAD R1, A R1 \leftarrow M[A] LOAD R2, B R2 \leftarrow M[B] LOAD R3, C R3 \leftarrow M[C] LOAD R4, D R4 \leftarrow M[D] ADD R1, R1, R2 R1 \leftarrow R1 + R2 ADD R3, R3, R4 R3 \leftarrow R3 + R4 MUL R1, R1, R3 R1 \leftarrow R1 * R3 STORE X, R1 M[X] \leftarrow R1

8.3 INSTRUCTION CYCLE(FETCH – EXECUTE- DECODE-RELOAD CYCLE)

Once a computer has been powered on it performs a continuous cycle of the following:

a. Fetch next instruction from memory

- b. Decode the instruction
- c. Execute the instruction

An instruction as the name instructs the computer what to do. In simple terms, every line of a program that we as users write instructs the computer to perform a series of operations.

What is Fetch Cycle: In fetch cycle the next instruction is fetched from the memory address that is currently stored in the Program Counter (PC), and stored in the Instruction register (IR). At the end of the fetch operation, the PC points to the next instruction that will be read at the next cycle.



Fig. 8.6: Steps of Instruction Cycle

Fetch Cycle Steps

- 1. The address in the CPU register IP is transmitted via the address bus to the memory unit's MAR: IP \rightarrow MAR
- 2. IP is incremented to point at the next program instruction, ready for the next cycle (IP point at individual **bytes** [= 8 bits] in memory):

IP ++

Memory selects addressed location and copies its contents onto the data bus: CPU loads received data into IR:

$$(MAR) \rightarrow IR$$

4. CPU starts decoding the instruction in IR



Fig. 8.7: Illustration of Fetch Cycle

The fetch cycle begins with retrieving the address stored in the **Program** Counter). The address stored in the PC is some valid address in the memory holding the instruction to be executed. (In case this address does not exist we would end up causing an interrupt or exception). The Central Processing Unit completes this step by fetching the instruction stored at this address from the memory and transferring this instruction to a special register – **Instruction Register (IR)** to hold the instruction to be executed. The program counter is incremented to point to the next address from which the new instruction is to be fetched.

Decode Cycle

The decode cycle is the decoder is used for interpreting the instruction that was fetched in the Cycle.

The operands are retrieved from the addresses if the need be.

- Part or all of the instruction in the IR is extracted to determine what is to be done
- · Part of the instruction may contain
 - Data
 - A memory address to get data from
 - A memory address to put data

Execute Cycle

This cycle as the name suggests, simply executes the instruction that was fetched and decoded.



Fig. 8.8: Illustrate the Execution Cycle

Example of Fetch-Decode-Execute-Reset Cycle

The following is an algorithm that shows the steps in the instruction cycle. At the end the cycle is reset and the algorithm repeated.

Step:1 Load the address that is in the program counter (PC) into the memory address register (MAR).

Increment the PC by 1.

Step:2 Load the instruction that is in the memory address given by the MAR into the memory data register (MDR).

Step: 3 Load the instruction that is now in the MDR into the current instruction register (CIR).

Step:4 Decode the instruction that is in the CIR.

Step:5 If the instruction is a jump instruction then

Step:6a. Load the address part of the instruction into the PC

b. Reset by going to step 1.

Step:7 Execute the instruction.

Step:8 Reset by going to step 1.

Steps 1 to 3 are the fetch part of the cycle. Steps 4 for decode part of cycle, 6a and 7 are the execute part of the cycle and steps 6b and 8 are the reset part of cycle.

Step 1 simply places the address of the next instruction into the memory address register so that the control unit can fetch the instruction from the right part of the memory. The program counter is then incremented by 1 so that it contains the address of the next instruction, assuming that the instructions are in consecutive locations.

The memory data register is used whenever anything is to go from the central processing unit to main memory, or vice versa. Thus the next instruction is copied from memory into the MDR and is then copied into the current instruction register.

Now that the instruction has been fetched the control unit can decode it and decide what has to be done. This is the execute part of the cycle. If it is an arithmetic instruction, this can be executed and the cycle restarted as the PC contains the address of the next instruction in order. However, if the instruction involves jumping to an instruction that is not the next one in order, the PC has to be loaded with the address of the instruction that is to be executed next. This address is in the address part of the current instruction, hence the address part is loaded into the PC before the cycle is reset and starts all over again.

8.3.1 Instruction cycle in Other Architectures of CPU

Using the above architecture for a microprocessor illustrates that basically an instruction can be in one of three phases. It could be being fetched (from memory), decode (by the control unit) or being executed (by the control unit). An alternative is to split the processor up into three parts, each of which handles one of the three stages. This would result in the situation

shown in Fig. 8.8, which shows how this process, known as pipelining, works.

Instruction 1

Instruction 2 Instruction 1

Instruction 3 Instruction 2 Instruction 1 Instruction 4 Instruction 3 Instruction 2 Instruction 5 Instruction 4 Instruction 3

Fig. 8.8: illustrate execution of Instruction in Pipe-Lining

This helps with the speed of throughput unless the next instruction in the pipe is not the next one that is needed. Suppose Instruction 2 is a jump to Instruction 10. Then Instructions 3, 4 and 5 need to be removed from the pipe and Instruction 10 needs to be loaded into the fetch part of the pipe. Thus, the pipe will have to be cleared and the cycle restarted in this case. The result is shown in Fig. 8.9

Instruction 1

Instruction 2 Instruction 1

Instruction 3 Instruction 2 Instruction 1

Instruction 4 Instruction 3 Instruction 2

Instruction 10

Instruction 11 Instruction 10

Instruction 12 Instruction 11 Instruction 10

Fig.8.9 Illustrate the jumping of Instruction 2 to Instruction 10

8.4 GLOSSARY

Three-address Instruction takes the form operation add-1, add-2, add-3. In this form, each of add-1, add-2, and add-3 refers to a register or to a memory location.

Two-address Instruction takes the form operation add-1, add-2. In this form, each of add-1 and add-2 refers to a register or to a memory location.

One-address Instruction takes the form ADD R1.

One-and-half Address Instruction. Between the two- and the one-address

Zero-address Instructions. These are the instructions that use stack operation.

Immediate Mode the value of the operand is (immediately) available in the instruction itself.

Direct (Absolute) Mode: The address of the memory location that holds the operand is included in the instruction

Indirect Mode: what is included in the instruction is not the address of the operand, but rather a name of a register

Indexed Mode: the address of the operand is obtained by adding a constant to the content of a register, called the index register

Relative Addressing: is the same as indexed addressing except that the Program Counter (PC) replaces the index register.

Instruction Format: It is the function of the control unit within the CPU to interpret each instruction code

Fetch Cycle: Next instruction is fetched from the memory address that is currently stored in the Program Counter (PC), and stored in the Instruction register (IR)

Execute Cycle: Fetched & Decoded Instruction is executed

8.5 REVIEW QUESTIONS

- Q.1 What are various addressing Modes discuss Direct, In-Direct and Indexed Modes.
- **Q.2** Discuss with Example:
 - (a) Three Address
 - (b) Two Address
 - (c) One & Half Address Address
 - (d) One Address
 - (e) Zero Address
- Q.3 What do you understand with Instruction Format? Write various types of Instructions.
- Q.4 Discuss the Fetch-Decode-Execution cycle with suitable Example.
- Q.5 Differentiate between : Direct and In-direct Addressing Mode.

Chapter 9

I/O Techniques and Memory Hierarchy

9.0 OBJECTIVES

After going through this chapter you should able to understand the concepts of:

- I/O Modules
- Data Transfer Technique- Programmed I/O, Interrupt Driven I/O,DMA
- DMA: Controller, DMA Transfer
- · Memory Hierarchy and its Needs
- Main Memory-RAM,ROM
- RAM:SRAM,DRAM
- ROM:PROM,EPROM,EEPROM
- Cache Memory
- Secondary Memory

9.1 EXTERNAL DEVICES

I/O operations are accomplished through external devices that provide a means of exchanging data between external environment and computer. An external device attaches to the computer by a link to an I/O module. An external device linked to an I/O module is called peripheral device or peripheral. External Devices can be categorized as

- 1. Human readable: suitable for communicating with computer user. For example video display terminals and printers.
- **2. Machine readable:** suitable for communicating with equipment. For example sensor, actuators used in robotics application.
- **3.** Communication: suitable for communicating with remote devices. They may be human readable device such as terminal and machine readable device such as another computer.

Following steps determine secure and fast data transfer

Control Signal – determines the function that the device will perform. e.g. send data to I/O module (READ or INPUT), receive data from I/O module (WRITE or OUTPUT), report status or perform some control function such as position a disk head.

Data Signal – send or receive the data from I/O module.

Status Signal - it indicates the status of signal. E.g. READY/NOT READY

- 1. Control Logic: associated with the device controls on specific operation as directed from I/O module.
- 2. Transducer: converts the data from electrical to other form of energy during output and from other forms of electrical during input.
- **3. Buffer:** is associated with transducer to temporarily hold data during data transmission from I/O module and external environment. Buffer size of 8 to 16 bits is common



Fig. 9.1: Control signal and Data Bus in I/O Module

9.2 INPUT VS OUTPUT MODULE

An external environment supplies the instruction and data; therefore, an input module is needed.

The main responsibility of input module will be to put the data in the form of signals that can be recognized by the system. Similarly, we need another component, which will report the results in the results in proper format and form. This component is called output module. These components are referred together as input/output (I/O) components.



Fig. 9.2: I/O Device Interfaces

In addition, to transfer the information, the computer system internally needs the system interconnections. Most common input/output devices are keyboard, monitor and printer, and the most common interconnection structure is the **Bus** structure.

Are these two components sufficient for a working computer? No, because input devices can bring instructions or data only sequentially and a program may not be executed sequentially as jump instructions are normally encountered in programming. In addition, more than one data elements may be required at a time. Therefore, a temporary storage area is needed in a computer to store temporarily the instructions and the data. This component is referred to as **Memory**.

It was pointed out by von- Neumann that the same memory can be used or storing data and instructions. In such cases the data can be treated as data on which processing can be performed, while instructions can be treated as data, which can be used for the generation of control signals.

The memory unit stores all the information in a group of memory cells, also called memory locations, as binary digits. Each memory location has a unique address and can be addressed independently. The contents of the desired memory locations are provided to the central processing unit by referring to the address of the memory location.

9.3 MODES OF TRANSFERS

There are basically THREE modes of data transfer between CPU and Memory:

- (i) Programmed I/O
- (ii) Interrupt Driven I/O
- (iii) DMA

9.3.1 Programmed I/O

The simplest strategy for handling communication between the CPU and an I/O module is programmed I/O. Using this strategy, the CPU is responsible for all communication with I/O modules, by executing instructions which control the attached devices, or transfer data.

For example, if the CPU wanted to send data to a device using programmed I/O, it would first issue an instruction to the appropriate I/O module to tell it to expect data. The CPU must then wait until the module responds before sending the data. If the module is slower than the CPU, then the CPU may also have to wait until the transfer is complete.

This can be very inefficient. Another problem exists if the CPU must read data from a device such as a keyboard. Every so often the CPU must issue an instruction to the appropriate I/O module to see if any keys have been pressed. This is also extremely inefficient.

Consequently this strategy is only used in very small microprocessor controlled devices.

9.3.2 Interrupt Driven I/O

Virtually all computers provide a mechanism 'y' which other modules (I/O, memory) may interrupt the normal processing of the CPU.

Program	Generated by some condition that occurs as a result of an instruction execution, such as arithmetic overflow, division by zero, attempt to execute an illegal machine instruction, and reference outside a
user's	
	allowed memory space.
Timer	Generated by a timer within the processor, This allows the operating system to perform certain functions on a regular basis.
I/O	Generated by an I/O controller, to signal normal completion of an operation or to signal a variety of error conditions.
Hardwarc Failure	Generated by a failurc such as power failurc or memory parity error.

Table 9.0: Lists the most common classes of interrupts

Interrupts are provided primarily as a way to improve processing efficiency. For example, most external devices are much slower than the processor. Support that Input/Output Instructions (I/O instructions) are used to transfer data between the computer and peripheral devices. The two basic I/O instructions used are the INPUT and OUTPUT instructions.

The INPUT instruction is used to transfer data from an input device to the processor. Examples of input devices include a keyboard or a mouse. Input devices are interfaced with a computer through dedicated input ports. Computers can use dedicated addresses to address these ports. Suppose that the input port through which a keyboard is connected to a computer carries the unique address 1000. Therefore, execution of the instruction INPUT 1000 will cause the data stored in a specific register in the interface between the keyboard and the computer, call it the input data register, to be moved into a specific register (called the accumulator) in the computer. Similarly, the execution of the instruction OUTPUT 2000 causes the data stored in the accumulator to be moved to the data output register in the output device whose address is 2000.

Advantages of Interrupt driven I/O over Progammed I/O Mode:

- Interrupt driven I/O strategy allows the CPU to carry on with its other operations until the module is ready to transfer data. When the CPU wants to communicate with a device, it issues an instruction to the appropriate I/O module, and then continues with other operations. When the device is ready, it will interrupt the CPU. The CPU can then carry out the data transfer as before.
- This also removes the need for the CPU to continually poll input devices to see if it must read any data. When an input device has data, then the appropriate I/O module can interrupt the CPU to request a data transfer.

How Interrupt driven I/O interrupt the CPU

An I/O module interrupts the CPU simply by activating a control line in the control bus. The sequence of events is as follows.

- 1. The I/O module interrupts the CPU.
- 2. The CPU finishes executing the current instruction.
- 3. The CPU acknowledges the interrupt.
- 4. The CPU saves its current state.
- 5. The CPU jumps to a sequence of instructions which will handle the interrupt.

The situation is somewhat complicated by the fact that most computer systems will have several peripherals connected to them. This means the computer must be able to detect which device an interrupt comes from, and to decide which interrupt to handle if several occur simultaneously. This decision is usually based **on interrupt priority**.

Some devices will require response from the CPU more quickly than others, for example, an

Interrupt from a disk drive must be handled more quickly than an interrupt from a keyboard.

Many systems use **multiple interrupt lines**. This allows a quick way to assign priorities to different devices, as the interrupt lines can have different priorities. However, it is likely that there will be more devices than interrupt lines, so some other method must be used to determine which device an interrupt comes from. Most systems use a system of **vectored interrupts**. When the CPU acknowledges an interrupt, the relevant device places a word of data (a vector) on the data bus. The vector identifies the device which requires attention, and is used by the CPU to look up the address of the appropriate interrupt handing routine.

Memory Mapped and Isolated I/O

Whether a system uses programmed or interrupt driven I/O, it must still periodically send instructions to the I/O modules. Two methods are used for to implement this:

- (a) Memory-mapped I/O and
- (b) Isolated I/O

With memory-mapped I/O, the I/O modules appear to the CPU as though they occupy locations in main memory. To send instructions or transfer data to an I/O module, the CPU reads or writes data to these memory locations. This will reduce the available address space for main memory, but as most modern systems use a wide address bus this is not normally a problem.

With isolated I/O, the I/O modules appear to occupy their own address space, and special instructions are used to communicate with them. This gives more address space for both memory and I/O modules, but will increase the total number of different instructions. It may also reduce the flexibility with which the CPU may address the I/O modules if less addressing modes are available for the special I/O instructions.

Multiple Interrupts

The above discussion so far has only discussed the occurrence of a single interrupt. However, that multiple interrupts can occur. For example, a program may be receiving data from a communications line and printing results.

The printer will generate an interrupt every time that it completes a print operation. The communication line controller will generate an interrupt every time a unit of data arrives. The unit could either be a single character or a block, depending on the nature of the communications

discipline. In any case, it is possible for a communication interrupt to occur while a printer interrupt is being processed.

Two approaches can be taken to dealing with multiple interrupts.

The first approach is to disable interrupts while an interrupt is being processed. A disabled interrupt simply means that the processor can and will ignore that interrupt request signal. If an interrupt occurs during this time, it generally remains pending and will be checked by the processor after the processor has enabled interrupts.

A second approach is to define priorities for interrupts and to allow an interrupt of higher priority to cause a lower-priority interrupt handler to be itself interrupted

Priority Interrupt

A priority interrupt establishes a priority to decide which condition is to be serviced first when two or more requests arrive simultaneously. The system may also determine which conditions are permitted to interrupt the computer while another interrupt is being serviced. Higher-priority interrupt levels are assigned to requests, which if delayed or interrupted, could have serious consequences.

Devices with high- speed transfers are given high priority, and slow devices receive low priority. When two devices interrupt the computer at the same time, the computer services the device, with the higher priority first. Establishing the priority of simultaneous interrupts can be done by software or hardware.

We can use a polling procedure to identify the highest-priority.

Daisy-Chaining Priority

The daisy-chaining method has a serial connection of all devices that request an interrupt. The device with the highest priority is kept in the first position, followed by lower-priority devices and so on. This method of connection is shown in Fig. 9.3.



Fig. 9.3: Daisy-chain priority interrupt

The interrupt request line is common to all devices and forms a wired logic connection. If any device has its interrupt signal in the low-level state, the interrupt line goes to the low-level state and enables the interrupt input in the CPU. When no interrupts are pending, the interrupt line stays in the high-level state and as a result CPU does not recognize any interrupt.

This is equivalent to a negative logic OR operation. The CPU responds to an interrupt request by enabling the interrupt acknowledge line.

This signal is received by device 1 at its PI (priority in) input. The acknowledge signal passes on to the next device through the PO (priority out) output only if device 1 is not requesting an

interrupt. If device I has a pending interrupt, it blocks the acknowledge signal from the next device by placing a 0 in the PO output. It then proceeds to insert its own interrupt vector address (VAD) into the data bus for the CPU to use during the interrupt cycle.

A device with PI=0 input generates a 0 in its PO output to inform the next-lower-priority device that the acknowledge signal has been blocked. A device that makes a request for an interrupt and has a I in its Pi input will intercept the acknowledge signal by placing a 0 in its PO output.

If the device does not have pending interrupts, it transmits the acknowledge signal to the next device by placing a 1 in its PO output. Thus the device with PI = 1 and PO = 0 is the one with the highest priority that is requesting an interrupt, and this device places its VAD on the data bus. The daisy chain arrangement gives the highest priority to the device that receives the interrupt acknowledge signal from the CPU. The farther the device is from the first position, the lower is its priority.

9.3.3 Direct Memory Access

Although interrupt driven I/O is much more efficient than program controlled I/O, all data is still transferred through the CPU. This will be inefficient if large quantities of data are being transferred between the peripheral and memory. The transfer will be slower than necessary, and the CPU will be unable to perform any other actions while it is taking place ,For this reason Direct Memory Access controller is used to bypass the CPU and provide a direct connection between the peripherals and memory, thus transferring the data as fast as possible

DMA Controller

Many systems therefore use an additional strategy, known as direct memory access (DMA). DMA uses an additional piece of hardware - a DMA controller. The DMA controller can take over the system bus and transfer data between an I/O module and main memory without the intervention of the CPU. Whenever the CPU wants to transfer data, it tells the DMA controller the direction of the transfer, the I/O module involved, the location of the data in memory, and the size of the block of data to be transferred. It can then continue with other instructions and the DMA controller will interrupt it when the transfer is complete.

The CPU and the DMA controller cannot use the system bus at the same time, so some way must be found to share the bus between them. One of two methods is normally used.

Burst mode

The DMA controller transfers blocks of data by halting the CPU and controlling the system bus for the duration of the transfer. The transfer will be as quick as the weakest link in the I/O module/bus/ memory chain, as data does not pass through the CPU, but the CPU must still be halted while the transfer takes place.

Cycle stealing

The DMA controller transfers data one word at a time, by using the bus during a part of an instruction cycle when the CPU is not using it, or by pausing the CPU for a single clock cycle on each instruction. This may slow the CPU down slightly overall, but will still be very efficient.

- Channel I/OThis is a system traditionally used on mainframe computers, but is becoming more common on smaller systems. It is an extension of the DMA concept, where the DMA controller becomes a full-scale computer system itself which handles all communication with the I/O modules.
- **2.** I/O Interfaces The interface of an I/O module is the connection to the peripheral(s) attached to it. The interface handles synchronisation and control of the peripheral, and the actual transfer of data. For example, to send data to a peripheral, the sequence of events would be as follows.
 - (a) The I/O module sends a control signal to the peripheral requesting permission to send data.
 - (b) The peripheral acknowledges the request.
 - (c) The I/O module sends the data (this may be either a word at a time or a block at a time depending on the peripheral).
 - (d) The peripheral acknowledges receipt of the data. This process of synchronisation is known as handshaking.

The internal buffer allows the I/O module to compensate for some of the difference in the speed at which the interface can communicate with the peripheral, and the speed of the system bus.

I/O interfaces can be divided into two main types.

- **3. Parallel interfaces** There are multiple wires connecting the I/O module to the peripheral, and bits of data are transferred simultaneously, as they are over the data bus. This type of interface is used for high speed peripherals such as disk drives.
- **4.** Serial interfacesOnly a single wire connects the I/O module to the peripheral, and data must be transferred one bit at a time. This is used for slower peripherals such as printers and keyboards.
- **5. I/O Function**Thus far, we have discussed the operation of the computer a s controlled by the CPU, and we have looked primarily at the interaction of CPU and memory. The discussion has only alluded to the role of the I/O component. An I/O module can exchange data directly with the CPU. Just as the CPU can initiate a read or write with memory, designating the address of a specific location, the CPU can also read data form or write data to an I/O module. In this latter case, the CPU identifies a specific device that is controlled by a particular I/O module.

In some cases, it is desirable to allow I/O exchanges to occur directly with memory. In such a case, the **CPU grants** to an I/O module the authority to read from or write to memory, so that the I.O memory transfer can occur without tying up the CPU. During such a transfer, the I/O module issues read or write commands to memory, relieving the CPU of responsibility for the exchange. This operation is known as direct memory access (DMA), an it will be examined in detail in chapter 6. For now, all that we need to know is that the interconnection structure of the computer may need to allow for direct memory – I/O interaction. This section introduces the concepts of input/output devices, modules and interfaces. It considers the various strategies used for communication between the CPU and I/O modules, and the interface between an I/O module and the device(s) connected to it.

DMA Transfer

There are three independent channels for DMA transfers. Each channel receives its trigger for the transfer through a large multiplexer that chooses from among a large number of signals. When these signals activate, the transfer occurs. The DMAxTSELx bits of the DMA Control Register 0 (DMACTL0). The DMA controller receives the trigger signal but will ignore it under certain conditions. This is necessary to reserve thememory bus for reprogramming and non-maskable interrupts etc. The controller also handles conflicts for simultaneous triggers. The priorities can be adjusted using the DMA Control Register 1 (DMACTL1). When multiple triggers happen simultaneously, they occur in order of module priority. The DMA trigger is then passed to the module whose trigger activated. The DMA channel will copy the data from the starting memorylocation or block to the destination memory location or block. There are many variations on this, and they are controlled by the DMA Channel x Control Register

(DMAxCTL):Single Transfer - each trigger causes a single transfer. The module will disable itself when DMAxSZ number of transfers have occurred (setting it to zero prevents transfer).

The DMAxSA and DMAxDA registers set the addresses to be transferred to and from.

The DMAxCTL register also allows these addresses to be incremented or decremented by 1 or 2 bytes with each transfer. This transfer halts the CPU.

Block Transfer - an entire block is transferred on each trigger. The module disables itself when this block transfer is complete. This transfer halts the CPU, and will transfer each memory location one at a time. This mode disables the module when the transfer is complete.

Burst-Block Transfer - this is very similar to Block Transfer mode except that the CPU and the DMA transfer can interleave their operation. This reduces the CPU to 20% while the DMA is going on, but the CPU will not be stopped altogether. The interrupt occurs when the block has completely transferred. This mode disables the module when the transfer is complete.

Repeated Single Transfer - the same as Single Transfer mode above except that the module is not disabled when the transfer is complete.

Repeated Block Transfer - the same as Block Transfer mode above except that the module is not disabled when the transfer is complete.

Repeated Burst-Block Transfer - the same as Burst Block Transfer mode above except that the module is not disabled when the transfer is complete.

Writing to flash requires setting the DMAONFETCH bit. If this is not done, the results of the DMA operation are "unpredictable." Also, the behavior and settings of the DMA module should only be modified when the module is disabled. The setting and triggers are highly configurable, allowing both edge and level triggering. The variety of settings is detailed in the DMA chapter of the users guide. Also, it is important to note that interrupts will not be acknowledged during the DMA transfer because the CPU is not active. Each DMA channel has its own flag, but the interrupt vector is shared with the DAC. This necessitates some software checking to handle interrupts with both modules enabled.

9.4 MEMORY HIERARCHY AND ITS NEED MEMORY

Overview

In this section we discusses the memory hierarchy - the different types and performance levels of memory found on a typical 80x86 computer system. Many programmers tend to view memory as this big nebulous block of storage that holds values for future use. From a semantic point of view, this is a reasonable view. However, from a performance point of view there are many different kinds of memory and using the wrong one or using one form improperly can have a dramatically negative impact on the performance of a program. This chapter discusses the memory hierarchy and how to best use it within your programs.

9.5 THE MEMORY HIERARCHY

Most modern programs can benefit greatly from a large amount of very fast memory. A physical reality, however, is that as a memory device gets larger, it tends to get slower. For example, cache memories are very fast but are also small and expensive. Main memory is inexpensive and large, but is slow.

The memory hierarchy is a mechanism of comparing the cost and performance of the various places we can store data and instructions.



Fig. 9.4: The Memory Hierarchy

In the Fig 9.4 memory hierarchy is shown here at the top level of the memory hierarchy are the CPU's **General Purpose Registers**. The registers provide the fastest access to data possible on the 80x86 CPU. The register file is also the smallest memory object in the memory hierarchy (with just eight general purpose registers available).

Working our way down, the Level **One Cache system** is the next highest performance subsystem in the memory hierarchy. On the 80x86 CPUs, the Level One Cache is provided on-chip by Intel and cannot be expanded. The size is usually quite small (typically between 4Kbytes and 32Kbytes), though much larger than the registers available on the CPU chip. Although the Level One Cache size is fixed on the CPU and you cannot expand it, the cost per byte of cache memory is much lower than that of the registers because the cache contains far more storage than is available in all the combined registers.

The Level Two Cache is present on some CPUs, on other CPUs it is the system designer's task to incorporate this cache (if it is present at all). For example, most Pentium II, III, and IV CPUs have a level two cache as part of the CPU package, but many of Intel's Celeron chips do no. The Level Two Cache is generally much larger than the level one cache (e.g., 256 or 512KBytes versus 16 Kilobytes). On CPUs where Intel includes the Level Two Cache as part of the CPU package, the cache is not expandable. It is still lower cost than the Level One Cache because we amortize the cost of the CPU across all the bytes in the Level Two Cache. On systems where the Level Two Cache is external, many system designers let the end user select the cache size and upgrade the size. For economic reasons, external caches are actually more expensive than caches that are part of the CPU package, but the cost per bit at the transistor level is still equivalent to the in-package caches.

Below the Level Two Cache system in the memory hierarchy falls the main memory subsystem. This is the general-purpose, relatively low-cost memory found in most computer systems. Typically, this is DRAM or some similar inexpensive memory technology.

Below main memory is the NUMA category. NUMA, which stands for <u>NonUniform Memory</u> <u>Access</u> is a bit of a misnomer here. NUMA means that different types of memory have different access times. Therefore, the term NUMA is fairly descriptive of the entire memory hierarchy. However here, we'll use the term NUMA to describe blocks of memory that are electronically similar to main memory but for one reason or another operate significantly slower than main memory. A good example is the memory on a video display card. Access to memory on video display cards is often much slower than access to main memory. Other peripheral devices that provide a block of shared memory between the CPU and the peripheral probably have similar access times as this video card example. Another example of NUMA includes certain slower memory technologies like Flash Memory that have significant slower access and transfers times than standard semiconductor RAM. We'll use the term NUMA in this chapter to describe these blocks of memory that look like main memory but run at slower speeds.

Most modern computer systems implement a **Virtual Memory scheme** that lets them simulate main memory using storage on a disk drive. While disks are significantly slower than main memory, the cost per bit is also significantly lower. Therefore, it is far less expensive (by three orders of magnitude) to keep some data on magnetic storage rather than in main memory. A Virtual Memory subsystem is responsible for transparently copying data between the disk and main memory as needed by a program.

File Storage also uses disk media to store program data. However, it is the program's responsibility to store and retrieve files data. In many instances, this is a bit slower than using Virtual Memory, hence the lower position in the memory hierarchy.

Below File Storage in the memory hierarchy comes Network Storage. At this level a program is keeping data on a different system that connects the program's system via a network. With Network Storage you can implement Virtual Memory, File Storage, and a system known as Distributed Shared Memory (where processes running on different computer systems share data in a common block of memory and communicate changes to that block across the network).

Virtual Memory, File Storage, and Network Storage are examples of so-called *on-line memory subsystems*. Memory access via these mechanism is slower than main memory access, but when a program requests data from one of these memory devices, the device is ready and able to respond to the request as quickly as is physically possible. This is not true for the remaining levels in the memory hierarchy.

The Near-Line and Off-Line Storage subsystems are not immediately ready to respond to a program's request for data. An Off-Line Storage system keeps its data in electronic form (usually magnetic or optical) but on media that is not (necessarily) connected to the computer system while the program that needs the data is running. Examples of Off-Line Storage include **magnetic tapes, disk cartridges, optical disks, and floppy diskettes.** When a program needs data from an off-line medium, the program must stop and wait for a someone or something to mount the appropriate media on the computer system. This delay can be quite long.

Hard Copy storage is simply a print-out (in one form or another) of some data. If a program requests some data and that data is present only in hard copy form, someone will have to manually enter the data into the computer. Paper (or other hard copy media) is probably the least expensive form of memory, at least for certain data types.

Application of the concept

IO processor manages data transfers between auxiliary memory and main memory. The cache organization is concerned with the transfer of information between main memory and CPU. Each is involved with a different level in the memory hierarchy system. The main reason for having two or three levels of memory hierarchy is economics.



Fig.9.5: Memory Organization

As the storage capacity of the memory increases the cost per bit for storing binary information decreases and the access time of the memory becomes longer. Auxiliary memory has a large storage capacity, inexpensive but has low access speed compared to main memory. The cache memory is very small relatively expensive and has very high access speed. The overall goal of using a memory hierarchy is to obtain the highest possible average access speed while minimizing the total cost of the entire memory system.

The memory hierarchy in most computers is:

- 1. Processor Registers fastest possible access (usually 1 CPU cycle), only hundreds of bytes in size
- 2. Level 1 (L1) cache often accessed in just a few cycles, usually tens of kilobytes
- 3. Level 2 (L2) cache higher latency than L1 by $2 \times$ to $10 \times$, often 512 KiB or more.

- **4. Main Memory -** may take hundreds of cycles, but can be multiple gigabytes. Access times may not be unifor m, in the case of a NUMA machine.
- 5. Disk Storage millions of cycles latency if not cached, but very large
- 6. Tertiary Storage several seconds latency, can be huge

9.6 MAIN MEMORY

Main memory is the second major subsystem in a computer. It consists of a collection of storage locations, each with a unique identifier, called an address. Data is transferred to and from memory in groups of bits called words.

A word can be a group of 8 bits, 16 bits, 32 bits or 64 bits (and growing).

If the word is 8 bits, it is referred to as a byte. The term "byte" is so common in computer science that sometimes a 16-bit word is referred to as a 2-byte word, or a 32-bit word is referred to as a 4-byte word.



Fig. 9.6: Main Memory Addressing

Details

Main memory is a temporary area for holding data, instructions, and information.

Main Memory is also known as main store or primary storage. The main store (main memory) is needed:

- To store the program currently being executed
- To hold data produced as the program is run
- To hold other data such as the contents of the screen. The backing store is needed:
- · For long-term storage of data and programs
- For data and programs where there is not enough room in the main store

Address Space AND Memory Address

To access a word in memory requires an identifier. Although programmers use a name to identify a word (or a collection of words), at the hardware level each word is identified by an address. The total

number of uniquely identifiable locations in memory is called the **address space**. For example, a memory with 64 kilobytes and a word size of 1 byte has an address space that ranges from 0 to 65,535.

- 1. Each memory location has an address
 - A unique number, much like a mailbox
- 2. RAM
 - Memory where any cell can be accessed independently
- 3. Referred to by number
 - Programming languages use a symbolic (named) address, such as Hours or Salary



Fig. 9.7: Memory cells arranged by address

RAM: Random Access Memory

- RAM is the main memory of a computer. It is used to temporarily store all information currently in use by the CPU.
- The RAM is a read-write memory thus information can be read and written to it. When you first turn your computer on, the RAM is empty since it is volatile. Volatile means that everything stored in RAM will be lost each time the computer is switched off.
- RAM will contain no data/information until you open or load a program. These programs are originally permanently stored in the external storage devices, like a hard disk or a floppy disk.
- When you open up the program, part of it is copied from the external device to the RAM, which is directly connected to the CPU. This is because if the CPU was to directly access this program from the external storage device, it would be extremely slow
- Computers use dynamic RAM as the main memory of the computer. This type of memory looses its content very quickly; therefore it needs to be refreshed thousands of times each second.
- The RAM is useful because it can feed information to the central processor at extremely high speeds. However, programs cannot be permanently stored on the RAM because
 - RAM, unlike hard drives, is **not big enough** to store all the programs a computer system contains.

- RAM is expensive
- RAM is volatile.
- A memory unit is a collection of storage cells together with associated circuits to transfer information in and out of storage and stores binary data in groups of bits called words
- · A word can represent an instruction code or alphanumeric characters
- Each word in memory is assigned an address from 0 to 2k -1, where k is the number of address lines
- A decoder inside the memory accepts an address opens the paths needed to select the bits of the specified word
- The memory capacity is stated as the total number of bytes that can be stored
 - Refer to the number of bytes using one of the following
 - K (kilo) = 2^{10} M (mega) = 2^{20}
 - G (giga) = 2^{30} 64K = 2^{10} , 2M = 2^{21} , and 4G = 2^{32}
- In random-access memory (RAM) the memory cells can be accessed for information from any desired random location
- The process of locating a word in memory is the same and requires an equal amount of time no matter where the cells are located physically in memory
- Communication between memory and its environment is achieved via data input and output lines, address selections lines, and control lines
 - The n data input lines provide the information to be stored in memory
 - The n data output lines supply the information coming out of memory
 - The k address lines provide a binary number of k bits that specify a specific word or location
 - The two control lines specify the direction of transfer either read or write



Fig. 9.8: Address line, I/O lines in Memory unit

Steps to Write to Memory

• Apply the binary address of the desired word into the address lineso Apply the data bits that are to be stored in memory on the data lineso Activate the write input

Steps to Read from Memory

- · Apply the binary address of the desired word into the address lines
- · Activate the read input

Further RAM may be classified in to TWO categories : Static RAM and Dynamic RAM

Static RAM (SRAM)

- Each cell stores bit with a six-transistor circuit Retains value indefinitely, as long as it is kept powered
- Relatively insensitive to disturbances such as electrical noise
- Faster and more expensive than DRAM



Fig. 9.9: Architecture of Static RAM

Explanation of SRAM

Storage cells in static RAM memory are made of flip-flops and therefore do not require refreshing in order to keep their data. This is in contrast to DRAM, discussed below. The problem with the use of flip-flops for storage cells is that each cell requires at least 6 transistors to build, and the cell holds only 1 bit of data. In recent years, the cells have been made of 4 transistors, which still is too many. The use of 4-transistor cells plus the use of CMOS technology has given birth to a high-capacity SRAM, but its capacity is far below DRAM.

Dynamic RAM (DRAM)

- · Each cell stores bit with a capacitor and transistor
- Value must be refreshed every 10-100 ms

- · Sensitive to disturbances
- · Slower and cheaper than SRAM



Fig. 9.10: Architecture of DRAM

Explanation of DRAM

Since the early days of the computer, the need for huge, inexpensive read/write memory has been a major preoccupation of computer designers. In 1970, Intel Corporation introduced the first dynamic RAM (random access memory). Its density (capacity) was 1024 bits and it used a capacitor to store each bit. Using a capacitor to store data cuts down the number of transistors needed to build the cell; however, it requires constant refreshing due to leakage. This is in contrast to SRAM (static RAM), whose individual cells are made of flip-flops. Since each bit in SRAM uses a single flip-flop, and each flip-flop requires 6 transistors, SRAM has much larger memory cells and consequently lower density. The use of capacitors as storage cells in DRAM results in much smaller net memory cell size.

ROM: Read only Memory

- The ROM is a Read-Only Memory. This means that you can only read its contents, but you cannot write over it and you cannot change or alter it in any way.
- ROM is used to store those programs essential for the normal running of a computer system such as the Bootstrap Loader. The **Bootstrap Loader** is a small program that is executed after pressing the 'on' button of a computer. Its function is to load Windows and run it; thereafter the user can start using the computer system.
- The ROM is also used to store certain information not needed to be changed. As one can imagine, ROM stores programs and information, which ideally are not lost when the computer is switched off, consequently ROM is **nonvolatile**. Non-volatile means that all information/programs stored on ROM will not be lost on switching off the computer.
- Note that any information or programs stored on ROM are permanently fixed during the manufacture of the ROM integrated circuit. ROMs are very cheap and reliable, but unfortunately, they are read-only.

- The binary information stored in a ROM is permanent during the hardware production-
- RAM is a general-purpose device whose contents can be altered
- The information in ROM forms the required interconnection pattern
- ROMs come with special internal electronic fuses that can be programmed for a specific configuration
- An m x n ROM is an array of binary cells organized into m words of n bits each
- A ROM has k address lines to select one of m words in memory and n output lines, one for each bit of the word
- May have one or more enable inputs for expansion
- The outputs are a function of only the present input (the address), so it is a combinational circuit constructed of decoders and OR gates
- Programs stored in ROM cannot be erased by viruses since they cannot be changed once they are produced.
 - **PROM (Programmable ROM)** is a memory Integrated Circuit which is manufactured blank so that the user is then able to store the desired programs on it. The disadvantage of PROM is that it can only be programmed once, if you make a mistake programming the chip, you will have to start all over.
 - **EPROM** stands for **Erasable and Programmable ROM**. Like PROM, EPROM is also manufactured blank so that the user can write in its contents, but it also has the additional feature of being erasable. To erase an EPROM, UV light is used. Thus the advantage of EPROM is that this kind of ROM can be reused.
 - EEPROM (Electrically Erasable Programmable ROM) EEPROM has several advantages over EPROM, such as the fact that its method of erasure is electrical and therefore instant, as opposed to the 20-minute erasure time required for UV-EPROM. In addition, in EEPROM one can select which byte to be erased, in contrast to UV-EPROM, in which the entire contents of ROM are erased. However, the main advantage of EEPROM is that one can program and erase its contents while it is still in the system board. It does not require physical removal of the memory chip from its socket. In other words, unlike UV-EPROM, EEPROM does not require an external erasure and programming device. To utilize EEPROM fully, the designer must incorporate the circuitry to program the EEPROM into the system board. In general, the cost per bit for EEPROM is much higher than for UV-EPROM.

9.7 CACHE MEMORY

Cache memory provides system designers with a way of exploiting high-speed processors without incurring the cost of large high-speed memory systems. The word cache is pronounced "cash" or "cash-ay" and is derived from the French word meaning hidden. Cache memory is hidden from the programmer and appears as part of the system's memory space. There's nothing mysterious about cache memory it's simply a quantity of very high-speed memory that can be accessed rapidly by the processor. Cache memory operates on exactly the same principle by locating frequently accessed information in the cache memory rather than in the much slower main memory.

Details

A block of cache memory sits on the processor's address and data buses in parallel with the much larger main memory. Note that the implication of parallel in the previous sentence is that data in the cache is also maintained in the main memory



Fig. 9.11: Typical Cache Organization



Fig. 9.12: Structure of Cache Memory
9.7.1 Principle of Locality

The probability of accessing the next item of data in memory isn't a random function. Because of the nature of programs and their attendant data structures, the data required by a processor is often highly clustered. This aspect of memories is called the locality of reference and makes the use of cache memory possible

The cache is usually filled from **main memory** when instructions or data are fetched into the CPU. Often the main memory will supply a wider data word to the cache than the CPU requires, to fill the cache more rapidly.

The amount of information which is replaces at one time in the cache is called the *line size* for the cache. This is normally the width of the data bus between the cache memory and the main memory. A wide line size for the cache means that several instruction or data words are loaded into the cache at one time, providing a kind of prefetching for instructions or data. Since the cache is small, the effectiveness of the cache relies on the following properties of most programs:

- **Temporal locality**: If a particular instruction or data item is used now, there is a good chance that it will be used again in the near future. Short loops are a common program structure, especially for the innermost sets of nested loops. This means that the same small set of instructions is used over and over. Generally, several operations are performed on the same data values, or variables.
- **Spatial locality**: If a particular instruction or data item is used now, there is a good chance that the instructions or data items that are located in memory immediately following or preceding this item will soon be used. most programs are highly sequential; the next instruction usually comes from the next memory location. Data is usually structured, and data in these structures normally are stored in contiguous memory locations.

9.7.2 Cache Operation – overview

- 1. CPU requests contents of memory location
- 2. Check cache for this data
- 3. If present, get from cache (fast)
- 4. If not present, read required block from main memory to cache
- 5. Then deliver from cache to CPU
- 6. Cache includes tags to identify which block of main memory is in each cache slot



Fig. 9.13: Cache Read Operation Flow-Chart

9.7.3 Cache Performance

Hit: data appears in some block in the upper level

- 1. Hit Rate: the fraction of memory access found in the upper level
- 2. Hit Time: Time to access the upper level which consists of Upper level access time + Time to determine hit/miss

Miss: data needs to be retrieve from a block in the lower level

Miss Rate = 1 - (Hit Rate)

- 1. Miss Penalty: time to replace a block from lower level, including time to replace in CPU:
 - Time to replace a block in the upper level + Time to deliver the block the processor

Access time : time to lower level = f (latency to lower level)

Transfer time : time to transfer block = f (Bandwidth between upper & lower levels) **Memory access time** = hit time + miss rate * miss penalty

- To improve performance, i.e., reduce memory time, we need to reduce:
 - 1. hit time,
 - 2. miss rate,
 - 3. miss penalty.

- As L1 caches are in the critical path of instruction execution,
- hit time is the most important parameter.
- When one parameter is improved, others might suffer

Compulsory miss

- block has never been in cache (during this execution of a program)
- always occurs on first access to a block

Capacity miss

- block was in cache, but was discarded to make room for other block
- reduces with cache size

Conflict miss

• block discarded because too many map to same set• reduces with level of associatively.

9.7.4 Cache Memory Organization

There are Three main different organization techniques used for cache memory.

- (i) DIRECT
- (ii) FULLY ASSOCITATIVE
- (iii) SET-ASSCIATIVE

The three techniques are discussed below. These techniques differ in two main aspects:

- 1. The criterion used to place, in the cache, an incoming block from the main memory.
- 2. The criterion used to replace a cache block by an incoming block (on cache full).

Direct Mapping

Direct Mapping This is the simplest among the three techniques. Its simplicity stems from the fact that it places an incoming main memory block into a specific fixed cache block location. The placement is done based on a fixed relation between the incoming block number, i, the cache block number, j, and the number of cache blocks, N:

j= i mod N

Example 1

Consider, for example, the case of a main memory consisting of 4K blocks, a cache memory consisting of 128 blocks, and a block size of 16 words. Figure 6.4 shows the division of the main memory and the cache according to the direct-mapped cache technique. As the figure shows, there are a total of 32 main memory blocks that map to a given cache block. For example, main memory blocks 0, 128, 256, 384, . . . ,3968 map to cache block 0. We therefore call the direct-mapping technique a many-to-one mapping technique.



Fig. 9.14: Mapping main memory blocks to cache blocks

The main advantage of the direct-mapping technique is its simplicity in determining where to place an incoming main memory block in the cache. Its main disadvantage is the inefficient use of the cache. This is because according to this technique, a number of main memory blocks may compete for a given cache block even if there exist other empty cache blocks. This disadvantage should lead to achieving a low cache hit ratio.

According to the direct-mapping technique the MMU interprets the address issued by the processor by dividing the address into three fields as shown in Figure 9.14.



Fig. 9.15: Direct Mapped Address Field

Fully Associative Mapping According to this technique, an incoming main memory block can be placed in any available cache block. Therefore, the address issued by the processor need only have two fields. These are the Tag and Word fields.

Facts of Fully Associative Mapping

- · A main memory block can load into any line of cache
- · Memory address is interpreted as tag and word
- · Tag uniquely identifies block of memory
- Every line's tag is examined for a match
- · Cache searching gets expensive

The first uniquely identifies the block while residing in the cache. The second field identifies the element within the block that is requested by the processor. The MMU interprets the address issued by the processor by dividing it into two fields as shown in Figure 9.15.



Fig. 9.16: Associative-mapped address fields

The main advantage of the associative-mapping technique is the **efficient use of the cache**. This stems from the fact that there exists no restriction on **where to place incoming main memory blocks**. Any unoccupied cache block can potentially be used to receive those incoming main memory blocks.

The main disadvantage of the technique, however, is the **hardware overhead required to perform the associative search** conducted in order to find a match between the tag field and the tag memory

A compromise between the simple but inefficient direct cache organization and the involved but efficient associative cache organization can be achieved by conducting the search over a limited set of cache blocks while knowing ahead of time where in the cache an incoming main memory block is to be placed.

This is the basis for the set-associative mapping technique explained below

Set-Associative Mapping In the set-associative mapping technique, the cache is divided into a number of sets. Each set consists of a number of blocks. A given main memory block maps to a specific cache set based on the equation **s=i MOD** S, where S is the number of sets in the cache, i is the main memoryblock number, and s is the specific cache set to which block i maps.

However, an incoming block maps to any block in the assigned cache set. Therefore, the address issued by the processor is divided into three distinct fields. These are the **Tag**, **Set**, **and Word fields**.

The Set field is used to uniquely identify the specific cache set that ideally should hold the targeted block. The Tag field uniquely identifies the targeted block within the determined set. The Word field identifies the element (word) within the block that is requested by the processor.

According to the set-associative mapping technique, the MMU interprets the address issued by the processor by dividing it into three fields as shown in Figure .9.16.



Fig. 9.17: Set Associative Memory

An overall qualitative comparison among the three mapping techniques is shown in Table9.3 Owing to its moderate complexity and moderate cache utilization, the set-associative technique is used in the Intel Pentium line of processors.

Mapping technique	Similicity	Associative tage search	Expected cache utilization	Raplacement technique
Direct	Yes	None	Low	Not needed
Associative	No	Involved	High	Yes
Set-associative	Moderate	Moderate	Moderate	Yes

Table. 9.3: Comparison Among Cache Mapping Techniques

9.7.5 Cache Write

Cache memories normally allow one of two things to happen when data is written into a memory location for which there is a value stored in cache:

- Write through cache both the cache and main memory are updated at the same time. This may slow down the execution of instructions which write data to memory, because of the relatively longer write time to main memory. Buffering memory writes can help speed up memory writes if they are relatively infrequent, however.
- Write back cache here only the cache is updated directly by the CPU; the cache memory controller marks the value so that it can be written back into memory when the word is removed from the cache. This method is used because a memory location may often be altered several times while it is still in cache without having to write the value into main memory. This method is often implemented using an "ALTERED" bit in the cache. The ALTERED bit is set whenever a cache value is written into by the processor. Only if the ALTERED bit is set is it necessary to write the value back into main memory (*i.e.*, only values which have been altered must be written back into main memory). The value should be written back immediately before the value is replaced in the cache.

9.8 SECONDRY MEMORY

You are now clear that the operating speed of primary memory or main memory should be as fast as possible to match with the CPU speed. These high-speed storage devices are very expensive and hence the cost per unit of storage is also very high. Again the storage capacity of the main memory is also very limited. Often it is necessary to store hundreds of millions of bytes of data for the CPU to process. Therefore additional memory is required in all the computer systems. This memory is called auxiliary storage, backup storage or secondary storage. In this type of memory the cost per bit of storage is low. However, the operating speed is slower than that of the primary storage. Huge volume of data are stored here on permanent basis and transferred to the primary storage as and when required. Most widely used secondary storage devices are

- magnetic tapes,
- floppy disk,
- magnetic disk,
- optical disks.

Magnetic Tape

Magnetic Tape: Magnetic tapes are used for large computers like mainframe computers where large volume of data is stored for a longer time. In PC also you can use tapes in the form of cassettes. The storage of data in tapes is inexpensive. Tapes consist of magnetic materials that store data permanently. It can be 12.5 mm to 25 mm wide plastic film-type and 500 meter to 1200 meter long, which is coated with magnetic material. The tape unit is connected to the central processor and information is fed into or read from the tape through the processor. It is similar to a cassette tape recorder.

Advantages of Magnetic Tape

- 1. Compact: A 10-inch diameter reel of tape is 2400 feet long and is able to hold 800, 1600 or 6250 characters in each inch of its length. The maximum capacity of such tape is 180 million characters Thus data are stored much more compactly on tape.
- 2. Economical: The cost of storing data is very less as compared to other storage devices.
- 3. Fast: Copying of data is easier and fast.
- 4. Long term Storage and Re-usability: Magnetic tapes can be used for long term storage and a tape can be used repeatedly with out loss of data.

FLOPPY DISK DRIVE

Floppy Disks

floppy disk is a secondary storage device. It is a circular piece of plastic material coated with particles, which are magnetized. This thin plastic sheet is protected from outside by a plastic cover to prevent the sensitive data stored on them. The commonly used floppy disks are of 3.5 " diameter. Floppies are used to store data and transfer them from one computer to another. Due to their size and portability they are the most popular storage mediums in offices and at homes.





Floppy Disks Fig. 9.18: Floppy Disks

The data inside the floppies are stored in tracks and sectors. The entire floppy is divided into circular segments called tracks. Each track is given a unique number. The outermost track is referred as 0 and the track inner to them is 1 and so on. Each track is further divided into segments called sectors. The number of segments in each track has the same capacity. In a typical 3.5" floppy disk the number of tracks and sectors and their storage capacity is denoted below:

1.44 MB = 1.474560 bytes = 512 bytes X 2 sides = 80 tracks X 18sectors

Thus these floppy disks are called high-density disks as they can hold 1.44 MB data. The outer plastic cover has read / write hole covered by a metal sheet. This metal cover automatically opens when the floppy is inserted inside the floppy disk drive. If we wish to protect our floppy and don't want anyone to write his or her data then this read/write notch on one edge of the floppy disk should be closed. After this the floppy becomes write protected.

The following guidelines should be taken care off while handling with floppy disks:

- · Magnetized items should be kept away from them
- Never bend or fold them.
- The touching of its surface must be avoided.
- The floppies should not be heaped/stacked one over the other.
- Heavy objects should not be kept on the floppies.
- Floppies should be kept away from heat & moisture.
- Floppies must be kept in cases to prevent them from dust.
- Very often formatting of floppies should be avoided.

Hard Disk

A hard disk is fixed inside the cabinet of CPU (Central Processing Unit). It is made up of many rigid metal platters coated to store data magnetically. The hard disk rotates while recording data. This rotation speed is measured in the unit of **revolutions per minute (rpm)**. The normal speed of hard disks is 3600 revolutions per second. The read/write head of the hard disks moves across its surface. The storage capacity of the hard disks is many times more than the floppy disks



Fig. 9.19: Hard-Disk

Due to large storage capacity it is preferred to store all important data into the hard disks of the computers. The data stored in the hard disks are retrieved faster as compared to the floppy disks as they are installed inside the computers.

OPTICAL DISK

Optical Disk

With every new application and software there is greater demand for memory capacity. It is the necessity to store large volume of data that has led to the development of optical disk storage medium. Optical disks read and write the data using light and not the magnetization as in above storage devices. Optical disks can be divided into the following categories:

- 1. Compact Disk/Read Only Memory (CD-ROM): CD-ROM disks are made of reflective metals. CD-ROM is written during the process of manufacturing by high power laser beam. Here the storage density is very high, storage cost is very low and access time is relatively fast. Each disk is approximately 4 ¹/₂ inches in diameter and can have over 600 MB of data. As the CD-ROM can be read only we cannot write or make changes into the data contained in it.
- 2. Write Once, Read Many (WORM): The inconvenience that we cannot write anything onto a CD-ROM is avoided in WORM. A WORM allows the user to write data permanently on to the disk. Once the data is written it can never be erased without physically damaging the disk. Here data can be recorded from keyboard, video scanner, OCR equipment and other devices. The advantage of WORM is that it can store vast amount of data amounting to gigabytes (10' bytes). Any document in a WORM can be accessed very fast, say less than 30 seconds.
- 3. Erasable Optical Disk: These are optical disks where data can be written, erased and re-written. This makes use of a laser beam to write and re-write the data. These disks may be used as alternatives to traditional disks. Erasable optical disks are based on a technology known as magneto-optico (MO). To write a data bit on to the erasable optical disk the MO drive's laser beam heats a tiny, precisely defined point on the disk's surface and magnetizes it.

9.9 GLOSSARY

Control Signal – determines the function that the device will perform.

Data Signal – send or receive the data from I/O module.

Status Signal – it indicates the status of signal. E.g. READY/NOT READYProgrammed I/O: The simplest strategy for handling communication between the CPU and an I/O module

Interrupt Driven I/O: Interrupt the CPU when ever Transfer is required

DMA: Direct Memory Access: allow the data transfer without intervention of CPU

Direct Memory Access controller: is used to bypass the CPU and provide a direct connection between the peripherals and memory

Cache Memory: High Speed Memory, placed between CPU and Main Memory

Cache Organization: DIRECT, Fully Associative and Set-Associative

Main Memory: is semiconductor memory, High Speed Memory

RAM: Read Only Memory: Volatile nature

SRAM: Static RAM: Each cell stores bit with a six-transistor circuit Retains value indefinitely, as long as it is kept powered

DRAM: Dynamic RAM: Each cell stores bit with a capacitor and transistor and Value must be refreshed every 10-100 ms

ROM: Read Only Memory: Non-Volatile nature

PROM (Programmable ROM) is a memory Integrated Circuit which is manufactured blank so that the user is then able to store the desired programs on it.

EPROM stands for **Erasable and Programmable ROM**

EEPROM (Electrically Erasable Programmable ROM)

9.10 REVIEW QUESTIONS

- Q.1 How the external devices provides the facility of data exchanging?
- Q.2 Discuss the all three types of data transfer mode with their relative advantages and disadvantages of each.
- **Q.3** Discuss the need of Memory Hierarchy.
- Q.4 Explain the concept of cache memory in computer organization.
- Q.5 What is role of cache memory in effective Data Transferring?
- Q.6 Why DMA is Beneficial to other modes of Data Transfer?
- Q.7 Discuss Various features of SRAM, DRAM.
- Q.8 What is Role of DMA controller in Data Transfer?
- Q.9 Write relative advantages of Interrupt driven I/O mode.
- Q.10 Why Secondary Memory are placed in lower in Memory Hierarchy?
- Q.11 Discuss the cache organization in detail.

Q.12 Write Short Note On:-

- (i) Miss and Hit
- (ii) Cache Write
- (iii) SRAM vs DRAM
- (iv) I/O Module
- (v) Bus
- (vi) Burst Mode
- (vii) Multiple and Priory Interrupt
- (viii) Vectored Interrupt
- (ix) Memory Mapped Isolated I/O Interrupt
- (x) Types of ROM
- (xi) Types of Secondary Memory
- (xii) Daisy Chaining Priority
- (xiii) WORM
- (xiv) Control, Data Signal
- (xv) Cycle Stealing
- (xvi) Bootstrap Loader

UNIT-IV

Chapter 10

Concept of Parallelism

10.0 OBJECTIVES

After going through this chapter you should able to understand the concepts of:

- Concept of Parallelism
- · Goals of Parallelism:
- Use of Parallelism
- Techniques' of Concurrency
- Instruction Level Parallelism (ILP)
 - Pipelining
 - Superscalar
- Processor Level Parallelism(PLP)
 - Array Computer
 - Multiprocessor
- Need of Parallel Computing
- Amdahl's Law
- Memory Architecture of Parallel Computer
 - Shared Memory-UMA,NUMA
 - Distributed Memory
 - Hybrid-Distributed Shared Memory

10.1 INTRODUCTION TO PARALLELISM

Traditionally, computer software has been written for Serial Computation. To solve a problem, an algorithm is constructed and implemented as a **serial steam of instructions.** These instructions are executed on a central processing unit on one computer. Only one instruction may execute at a time—after that instruction is finished, the next is executed.



Fig:10.1: Parallel Computing in Computer

• The compute resources can include:

- A single computer with multiple processors;
- An arbitrary number of computers connected by a network;
- A combination of both.
- The computational problem usually demonstrates characteristics such as the ability to be:
 - Broken apart into discrete pieces of work that can be solved simultaneously;
 - Execute multiple program instructions at any moment in time;
 - Solved in less time with multiple compute resources than with a single compute resource.

10.1.1 Goals of Parallelism

- The purpose of parallel processing is to speedup the computer processing capability or in words, it increases the computational speed.
- Increases throughput, i.e. amount of processing that can be accomplished during a given interval of time.
- Improves the performance of the computer for a given clock speed.
- Two or more ALUs in CPU can work concurrently to increase throughput.
- The system may have two or more processors operating concurrently.

10.1.2 Uses of Parallelism

- Historically, parallelism has been considered to be "the high end of computing", and has been used to model difficult scientific and engineering problems found in the real world. Some examples:
 - Atmosphere, Earth, Environment
 - Physics applied, nuclear, particle, condensed matter, high pressure, fusion, photonics
 - Bioscience, Biotechnology, Genetics
 - Chemistry, Molecular Sciences

- Geology, Seismology
- Mechanical Engineering from prosthetics to spacecraft
- Electrical Engineering, Circuit Design, Microelectronics
- Computer Science, Mathematics
- Today, commercial applications provide an equal or greater driving force in the development of faster computers. These applications require the processing of large amounts of data in sophisticated ways. For example:
 - Databases, Data Mining
 - Oil exploration
 - Web Search Engines, Web Based Business Services
 - Medical imaging and Diagnosis
 - Pharmaceutical Design
 - Management of National and Multi-national Corporations
 - Financial and Economic Modeling
 - Advanced Graphics and Virtual Reality, Particularly in the Entertainment Industry
 - Networked Video and Multi-media Technologies
 - Collaborative Work Environments

10.1.3 Why Use Parallel Computing

- Save time and/or money: In theory, throwing more resources at a task will shorten its time to completion, with potential cost savings. Parallel clusters can be built from cheap, commodity components.
- Solve larger problems: Many problems are so large and/or complex that it is impractical or impossible to solve them on a single computer, especially given limited computer memory
- **Provide concurrency:** A single compute resource can only do one thing at a time. Multiple computing resources can be doing many things simultaneously.
- Use of non-local resources: Using computer resources on a wide area network, or even the Internet when local compute resources are scarce.
- Limits to serial computing: Both physical and practical reasons pose significant constraints to simply building ever faster serial computers:
 - **Transmission speeds** the speed of a serial computer is directly dependent upon how fast data can move through hardware. Absolute limits are the speed of light (30 cm/nanosecond) and the transmission limit of copper wire (9 cm/nanosecond). Increasing speeds necessitate increasing proximity of processing elements.
 - Limits to miniaturization processor technology is allowing an increasing number of transistors to be placed on a chip. However, even with molecular or atomic-level components, a limit will be reached on how small components can be.
 - **Economic limitations** it is increasingly expensive to make a single processor faster. Using a larger number of moderately fast commodity processors to achieve the same (or better) performance is less expensive.

10.1.4 Techniques of Concurrency

- Overlap: Execution of multiple operations by heterogenous functional units.
- Parallelism : Execution of multiple operations by homogenous functional units

Throughput Enhancement

A computer's performance is measured by the time taken for executing a program.

The program execution involves performing instruction cycles, which includes **Two** types of operations:

- Internal Micro-operations: performed inside the hardware functional units such as the processor, memory, I/O etc.
- **Transfer of Information:** between different functional hardware units for Instruction fetch, operand fetch, I/O operation etc.

Instruction Level Parallelism (ILP)

- Pipelining
- Superscalar

Processor Level Parallelism

- Array Computer
- Multiprocessor

10.2 AMDAHL'S LAW

• States that potential program speedup is defined by the **Fraction of code** (P) that can be parallelized:

speed up =
$$\frac{1}{p-0}$$

- If none of the code can be parallelized, P = 0 and the speedup = 1 (no speedup).
- If all of the code is parallelized, P = 1 and the speedup is infinite (in theory).
- If 50% of the code can be parallelized, maximum speedup = 2, meaning the code will run twice as fast.
- Introducing the number of processors performing the parallel fraction of work, the relationship can be modeled by:

speed up =
$$\frac{1}{\frac{P+S}{N}}$$

where P = parallel fraction, N = number of processors and S = serial fraction.

• It soon becomes obvious that there are limits to the scalability of parallelism. For example:

speedup									
N	P = .50	P = .90	P = .99						
10	1.82	5.26	9.17						
100	1.98	9.17	50.25						
1000	1.99	9.91	90.99						
10000	1.99	9.91	99.02						
100000	1.99	9.99	99.90						



Fig. 10.2: (A graphical representation of Amdahl's law. The speed-up of a program from parallelization is limited by how much of the program can be parallelized. For example, if 90% of the program can be parallelized, the theoretical maximum speed-up using parallel computing would be 10x no matter how many processors are used)

Some facts related to this rule are listed below

- 1. Amdahl's law, also known as Amdahl's argument, is named after computer architect Gene Amdahl, and is used to find the maximum expected improvement to an overall system when only part of the system is improved.
- 2. It is often used in **parallel computing** to predict the theoretical maximum speedup using multiple processors.
- 3. The speedup of a program using multiple processors in parallel computing is limited by the time needed for the sequential fraction of the program.
- 4. Amdahl's law is a model for the relationship between the expected speedup of parallelized implementations of an algorithm relative to the serial algorithm, under the assumption that the problem size remains the same when parallelized.

- 5. The law is concerned with the speedup achievable from an improvement to a computation that affects a proportion P of that computation where the improvement has a speedup of S. (For example, if an improvement can speed up 30% of the computation, P will be 0.3; if the improvement makes the portion affected twice as fast, S will be 2.)
 - Amdahl's law states that the overall speedup of applying the improvement will be:
 - Old Running Time/New Running Time = 1 /((1-P)+P/S)
 - To see how this formula was derived, assume that the running time of the old computation was 1, for some unit of time. The running time of the new computation will be the length of time the unimproved fraction takes, (1 " *P*), plus the length of time the improved fraction takes.
 - The length of time for the improved part of the computation is the length of the improved part's former running time divided by the speedup, making the length of time of the improved part P/S. The final speedup is computed by dividing the old running time by the new running time, which is what the above formula does.
 - In the case of parallelization, Amdahl's law states that if P is the proportion of a program that can be made parallel (i.e. benefit from parallelization), and $(1 \ P)$ is the proportion that cannot be parallelized (remains serial), then the maximum speedup that can be achieved by using N processors is :

1/(1-P)+P/N.

• P can be estimated by using the measured speedup SU on a specific number of processors NP using

Estimated= (1/SU - 1) / (1/NP-1).

• *P* estimated in this way can then be used in Amdahl's law to predict speedup for a different number of processors.

10.3 INSTRUCTION-LEVEL PARALLELISM (ILP)

- **Instruction-level parallelism** (ILP) is a measure of how many of the operations in a computer program can be performed simultaneously.
- Micro-architectural techniques that are used to exploit ILP include:
- Instruction pipelining where the execution of multiple instructions can be partially overlapped.
 SUPERSCALAR execution in which multiple execution units are used to execute multiple instructions in parallel. In typical superscalar processors, the instructions executing simultaneously
- instructions in parallel. In typical superscalar processors, the instructions executing simultaneously are adjacent in the original program order.
- A superscalar CPU architecture implements a form of parallelism called instruction-level parallelism within a single processor.
- It therefore allows faster CPU throughput than would otherwise be possible at a given clock rate.

Points to Remember

- A superscalar processor executes more than one instruction during a clock cycle by simultaneously dispatching multiple instructions to redundant functional units on the processor.
- Each functional unit is not a separate CPU core but an execution resource within a single CPU such as an arithmetic logic unit, a bit shifter, or a multiplier.

- Superscalar CPU is typically also pipelined.
- · Instructions are issued from a sequential instruction stream
- CPU hardware dynamically checks for data dependencies between instructions at run time (versus software checking at compile time)
- The CPU accepts multiple instructions per clock cycle
- Pipelining and Superscalar architecture are considered different performance enhancement techniques.

Instruction Pipeline

- An instruction pipeline reads consecutive instructions from memory while previous instructions are being executed in other segments.
- Computer needs to process each instruction with the following sequence of steps.
 - Fetch the instruction from memory
 - Decode the instruction
 - Calculate the effective address
 - Fetch the operands from memory
 - Execute the instruction
 - Store the result in the proper place



Fig. 10.3: Various stages of Instruction Cycle

Four Segment Pipeline

1	FI	DA	FO	EX									
2		FI	DA	FO									
3			FI	DA									
4				FI	-	-	FI	DA	FO	EX			
5					-	-	-	FI	DA	FO	EX		
6									FI	DA	FO	EX	
7										FI	DA	FO	EX

Fig. 10.4: Vaious Instruction in Four Segmented Pipe-line

Pipeline Conflicts

- 1. Resource conflicts caused by access to memory by two segments at the same time. These may be resolved by using separate instruction and data memories.
- 2. Data Dependency conflicts arise when an instruction depends on the result of a previous instruction, but this result is not yet available.
- 3. Branch Difficulties arise from branch and other instructions that change the value of PC.

The superscalar technique is associated with several identifying characteristics (within a given CPU core):

- Instructions are issued from a sequential instruction stream.
 - CPU hardware dynamically checks for data dependencies between instructions at run time (versus software checking at compile time)
 - The CPU accepts multiple instructions per clock cycle.
- Available performance improvement from superscalar techniques is limited by Two key areas:
 - The degree of intrinsic parallelism in the instruction stream, i.e. limited amount of instruction-level parallelism, and
 - The complexity and time cost of the dispatcher and associated dependency checking logic.
 - The branch instruction processing.

10.4 PROCESSOR-LEVEL PARALLELISM (PLP)

• **Multiprocessing** is the use of two or more central processing units (CPUs) within a single computer system.

- The term also refers to the ability of a system to support more than **one processor and/or the ability to allocate tasks between them.**
- *Multiprocessing* sometimes refers to the execution of multiple concurrent software processes in a system as opposed to a single process at any one instant.
- The terms **multitasking or multiprogramming** are more appropriate to describe this concept, which is implemented mostly in **software**, whereas **multiprocessing** is more appropriate to describe the use of multiple **hardware CPUs**.
- A system can be both multiprocessing and multiprogramming, only one of the two, or neither of the two.
- In a **Multiprocessing** system, all CPUs may be equal, or some may be reserved for special purposes.
- In **Multiprocessing**, the processors can be used to execute a single sequence of instructions in multiple contexts
- In a Single Instruction Stream, Single Data Stream or SISD, one processor sequentially processes instructions, each instruction processes one data item.
- Single-Instruction, Multiple-Data or SIMD, often used in vector processing
- Multiple sequences of instructions in a single context multiple-instruction, single-data or MISD, used to describe pipelined processors.
- Multiple sequences of instructions in multiple contexts (multiple-instruction, multiple-data or MIMD.

Advantages of multiprocessor system are as follows:

- **Reduced Cost:** Multiple processors share the same resources. Separate power supply or mother board for each chip is not required. This reduces the cost.
- **Increased Reliability:** The reliability of system is also increased. The failure of one processor does not affect the other processors though it will slow down the machine. Several mechanisms are required to achieve increased reliability. If a processor fails, a job running on that processor also fails. The system must be able to reschedule the failed job or to alert the user that the job was not successfully completed.
- **Increased Throughput:** An increase in the number of processes completes the work in less time. It is important to note that doubling the number of processors does not halve the time to complete a job. It is due to the overhead in communication between processors and contention for shared resources etc

1.5 PARALLEL COMPUTER MEMORY ARCHITECTURES

10.5.1Shared Memory

General Characteristics

- Shared memory parallel computers vary widely, but generally have in common the ability for all processors to access all memory as global address space.
- Multiple processors can operate independently but share the same memory resources.
- Changes in a memory location effected by one processor are visible to all other processors.
- Shared memory machines can be divided into Two main classes based upon memory access times: *UMA* and NUMA



Fig.10.5: Shared Memory (UMA)

Uniform Memory Access (UMA)

- Most commonly represented by Symmetric Multiprocessor(SMP) Machines
- Identical processors
- · Equal access and access times to memory
- Sometimes called **CC-UMA Cache Coherent UMA**. Cache coherent means if one processor updates a location in shared memory, all the other processors know about the update. Cache coherency is accomplished at the hardware level.

Non-Uniform Memory Access (NUMA)

- Often made by physically linking two or more SMPs
- One SMP can directly access memory of another SMP
- Not all processors have equal access time to all memories
- · Memory access across link is slower
- If cache coherency is maintained, then may also be called CC-NUMA Cache Coherent NUMA



Fig.10.6: Shared Memory (NUMA)

Advantages

- · Global address space provides a user-friendly programming perspective to memory
- Data sharing between tasks is both fast and uniform due to the proximity of memory to CPUs

Disadvantages

- Primary disadvantage is the lack of scalability between memory and CPUs. Adding more CPUs can geometrically increases traffic on the shared memory-CPU path, and for cache coherent systems, geometrically increase traffic associated with cache/memory management.
- Programmer responsibility for synchronization constructs that ensure "correct" access of global memory.
- Expense: it becomes increasingly difficult and expensive to design and produce shared memory machines with ever increasing numbers of processors.

10.5.2 Distributed Memory

General Characteristics

• Like shared memory systems, distributed memory systems vary widely but share a common characteristic. Distributed memory systems require a **communication network to connect inter-processor memory.**





- Processors have their **own local memory.** Memory addresses in one processor do not map to another processor, so there is no concept of global address space across all processors.
- Because each processor has its own local memory, it operates independently. Changes it makes to its local memory have no effect on the memory of other processors. Hence, the concept of cache coherency does not apply.
- When a processor needs access to data in another processor, it is usually the task of the programmer to explicitly define how and when data is communicated. Synchronization between tasks is likewise the programmer's responsibility.
- The network "fabric" used for data transfer varies widely, though it can can be as simple as Ethernet.

Advantages

- Memory is scalable with number of processors. Increase the number of processors and the size of memory increases proportionately.
- Each processor can rapidly access its own memory without interference and without the overhead incurred with trying to maintain cache coherency.
- · Cost effectiveness: can use commodity, off-the-shelf processors and networking.

Disadvantages

- The programmer is responsible for many of the details associated with data communication between processors.
- It may be difficult to map existing data structures, based on global memory, to this memory organization.
- Non-uniform memory access (NUMA) times

10.5.3 Hybrid Distributed-Shared Memory

• The largest and fastest computers in the world today employ both shared and distributed memory architectures.





- The shared memory component is usually a cache coherent SMP machine. Processors on a given SMP can address that machine's memory as global.
- The distributed memory component is the networking of multiple SMPs. SMPs know only about their own memory not the memory on another SMP. Therefore, network communications are required to move data from one SMP to another.
- Current trends seem to indicate that this type of memory architecture will continue to prevail and increase at the high end of computing for the foreseeable future.
- Advantages and Disadvantages: whatever is common to both shared and distributed memory architectures.

10.6 DESIGN LIMITATION OF PARALLEL APPLICATIONS

In general, parallel applications are much more complex than corresponding serial applications, perhaps an order of magnitude. Not only do you have multiple instruction streams executing at the same time, but you also have data flowing between them.

- The costs of complexity are measured in programmer time in virtually every aspect of the software development cycle:
 - Design
 - Coding
 - Debugging
 - Tuning
 - Maintenance
- Adhering to "good" software development practices is essential when when working with parallel applications especially if somebody besides you will have to work with the software.

Some General Parallel Terminology

Some of the more commonly used terms associated with parallel computing are listed below:-

Task

A logically discrete section of computational work. A task is typically a program or program-like set of instructions that is executed by a processor.

Parallel Task

A task that can be executed by multiple processors safely (yields correct results)

Serial Execution

Execution of a program sequentially, one statement at a time. In the simplest sense, this is what happens on a one processor machine. However, virtually all parallel tasks will have sections of a parallel program that must be executed serially.

Parallel Execution

Execution of a program by more than one task, with each task being able to execute the same or different statement at the same moment in time.

Pipelining

Breaking a task into steps performed by different processor units, with inputs streaming through, much like an assembly line; a type of parallel computing.

Shared Memory

From a strictly hardware point of view, describes a computer architecture where all processors have direct (usually bus based) access to common physical memory. In a programming sense, it describes a model where parallel tasks all have the same "picture" of memory and can directly address and access the same logical memory locations regardless of where the physical memory actually exists.

Symmetric Multi-Processor (SMP)

Hardware architecture where multiple processors share a single address space and access to all resources; shared memory computing.

Distributed Memory

In hardware, refers to network based memory access for physical memory that is not common. As a programming model, tasks can only logically "see" local machine memory and must use communications to access memory on other machines where other tasks are executing.

Communications

Parallel tasks typically need to exchange data. There are several ways this can be accomplished, such as through a shared memory bus or over a network, however the actual event of data exchange is commonly referred to as communications regardless of the method employed.

Synchronization

The coordination of parallel tasks in real time, very often associated with communications. Often implemented by establishing a synchronization point within an application where a task may not proceed further until another task(s) reaches the same or logically equivalent point.

Synchronization usually involves waiting by at least one task, and can therefore cause a parallel application's wall clock execution time to increase.

Granularity

In parallel computing, granularity is a qualitative measure of the ratio of computation to communication.

- Coarse: relatively large amounts of computational work are done between communication events
- Fine: relatively small amounts of computational work are done between communication events

Observed Speedup

Observed speedup of a code which has been parallelized, defined as:

wall-clock time of serial execution

wall-clock time of parallel execution

One of the simplest and most widely used indicators for a parallel program's performance.

Parallel Overhead

The amount of time required to coordinate parallel tasks, as opposed to doing useful work. Parallel overhead can include factors such as:

- · Task start-up time
- Synchronizations
- Data communications
- Software overhead imposed by parallel compilers, libraries, tools, operating system, etc.
- Task termination time

Massively Parallel

Refers to the hardware that comprises a given parallel system - having many processors. The meaning of "many" keeps increasing, but currently, the largest parallel computers can be comprised of processors numbering in the hundreds of thousands.

Embarrassingly Parallel

Solving many similar, but independent tasks simultaneously; little to no need for coordination between the tasks.

Scalability

Refers to a parallel system's (hardware and/or software) ability to demonstrate a proportionate increase in parallel speedup with the addition of more processors. Factors that contribute to scalability include:

- Hardware particularly memory-cpu bandwidths and network communications
- · Application algorithm
- Parallel overhead related
- Characteristics of your specific application and coding

Multi-core Processors

Multiple processors (cores) on a single chip.

Cluster Computing

Use of a combination of commodity units (processors, networks or SMPs) to build a parallel system.

Supercomputing / High Performance Computing

Use of the world's fastest, largest machines to solve large problems

10.7 GLOSSARY

Parallelism: Executing two or more operations at the same time is known as Parallelism.

Parallel computing is the simultaneous use of multiple compute resources to solve a computational problem

Amdahl's Law This rule states that a small portion of the program which cannot be parallelized will limit the overall speed-up available from parallelization

Instruction-level parallelism (ILP) is a measure of how many of the operations in a computer program can be performed simultaneously

Superscalar in which multiple execution units are used to execute multiple instructions in parallel

Instruction Pipeline reads consecutive instructions from memory while previous instructions are being executed in other segments

Multiprocessing is the use of two or more central processing units (CPUs) within a single computer system

Task : It is typically a program or program-like set of instructions that is executed by a processor.

Parallel Task A task that can be executed by multiple processors safely (yields correct results)

Serial Execution: Execution of a program sequentially, one statement at a time.

Parallel Execution: Execution of a program by more than one task, with each task being able to execute the same or different statement at the same moment in time.

Pipelining: Breaking a task into steps performed by different processor units, with inputs streaming through, much like an assembly line; a type of parallel computing.

Shared Memory: From a strictly hardware point of view, describes a computer architecture where all processors have direct (usually bus based) access to common physical memory.

Symmetric Multi-Processor (SMP): where multiple processors share a single address space and access to all resources

Distributed Memory: refers to network based memory access for physical memory that is not common.

Parallel Overhead: The amount of time required to coordinate parallel tasks.

Massively Parallel: Refers to the hardware that comprises a given parallel system - having many processors. **Embarrassingly Parallel**: Solving many similar, but independent tasks simultaneously; little to no need for coordination between the tasks.

Scalability: Refers to a parallel system's ability to demonstrate a proportionate increase in parallel speedup with the addition of more processors.

Multi-core Processors: Multiple processors (cores) on a single chip.

Cluster Computing: Use of a combination of commodity units (processors, networks or SMPs) to build a parallel system.

Supercomputing / High Performance Computing : Use of the world's fastest, largest machines to solve large problems

10.8 REVIEW QUESTIONS

Q.1 What is parallelism? How parallel computation is beneficial over serial computation?

Q.2 What are objectives/goals of parallelism implementation?

Q.3 What are main two types of parallelism can be implemented in computer organization?

Q.4 How Instruction Level Parallelism (ILP) implemented?

Q.5 Discuss processor level implementation with overview of multi-processor system.

Q.6 Explain implementation of pipe-lined and Superscalar architecture.

Q.7 Write the Memory distribution in parallel architecture.

Q.8 Write the various designing issues of parallel architecture.

Q.9 Explain and Discuss various categories of Memory in parallel computer.

Q.10 Differentiate Between

(i) ILP Vs PLP

(ii) UMA Vs NUMA

- (iii) Serial Vs Parallel Computation
- (iv) Pipe-lining Vs Super scaling

Q.11 Write Short Notes:

- (i) Performance Enhancement in Parallel Computing
- (ii) Multi Processor Systems
- (iii) Distributed Memory
- (iv) Superscalar Execution
- (v) limitations of Serial Computing
- (vi) Amdahl Law for Parallelism

Chapter 11

Instruction Code and Instruction Format

11.0 OBJECTIVE

After going through this chapter you should able to understand the concepts of:

- Concept of Instruction Code
 - Operation Part
 - Memory Address
 - Instruction Set
- Various Categories of Instruction
 - Data Transfer Instructions
 - Arithmetic Instructions
 - · Logical and bit Manipulation Instructions
 - String Transfer Instructions
 - Processor Execution Instructions
 - Processor Control Instructions
- Timing Control
- Instruction Format
 - General Instruction Format
 - Three Instruction Format
 - R-Type
 - J-Type
 - I-Type

11.1 INTRODUCTION

We all know that without our instructions a computer can do nothing. Hence we need to instruct the computer to perform a specific operation.

(a) The collection of bits that instruct the computer to perform a specific operation is called an **Instruction Code.**

- (b) Operation part is the most basic part of an instruction code. The operation code of an instruction is a group of bits that define such operations as **add**, **subtract**, **multiply**, **shift and complement**.
- (c) The total number of operations available in the computer determines the number of bits required for the operation code of an instruction. The operation code must consist of at least n bits for a given 2ⁿ (or less) distinct operations.
- (d) An **'operation'** is a binary code that instructs the computer to perform a specific operation. The control unit gets the instruction from memory and interprets the operation code bits. It then issues a sequence of control signals to initiate micro-operations in internal computer registers. For every operation code, the control issues a sequence of micro-operations required for the hardware implementation of the specified operation.

This operation should be performed on some data stored in processor registers or on the data stored in the memory. Hence an instruction code must specify the operation and the registers or the memory words where the operands are to be found, as well as the registers or the memory word where the operands are stored.

Memory words can be specified in instruction codes by their address. Processor registers can be specified by assigning to the instruction another binary code of K bits that specifies one of 2K registers. There are many variations for arranging the binary code of instructions. Each computer has its own particular instruction code format called its **Instruction Set**.

11.2 VARIOUS CATEGORIES OF INSTRUCTION

I. Data Transfer Instructions: Most of CPU Instructions are Data transfer Instructions. The data transfer instructions move data between memory and the general-purpose and segment registers. They also perform specific operations such as conditional moves, stack access, and data conversion.

PUSH — Copy specified word to top of stack.

POP — Copy word from top of stack to specific location.

PUSHA (80186/80188 only) — Copy all registers stack.

POPA (80186/80188 only) — Copy words f stack to all registers.

XCHG ————Exchange bytes or exchange words.

XLAT — Translate a byte in AL using a table in memory.

Simple input and output port transfer instructions

IN —Copy a byte or word from specified port to accumulator.

OUT- Copy a byte or word from accumulator specified port.

Special address transfer instructions

LEA - Load effective address of operand in specified register.

LDS — Load DS register and other specified register from memory.

LES — Load ES register and other specified register from memory.

Flag Transfer Instructions

LAHF Load (copy to) — AH with the low byte the flag register.

SAHF Store (copy) — AH register to low byte of register.

PUSHF — Copy flag register to top of stack.

POPF — Copy word at top of stack to flag register

II. Arithmetic Instructions: Arithmetic instructions perform basic binary integer computations on byte, word, and double word integers located in memory and/or the general purpose registers

ADD — Add specified byte to byte or specified word to word.

- ADC Add byte + byte + carry flag or word + word + carry flag.
- **INC** Increment specified byte or specified by 1.
- AAA ASCII adjust after addition.
- **DAA** Decimal (BCD) adjust after addition.
- SUB Subtract byte from byte or word from word.
- SBB Subtract byte and carry flag from byte word and carry flag from word.

DEC — Decrement specified byte or specified word by 1.

NEG Negate – invert each bit of a specified byte or word and add 1 (form 2's complement).

CMP Compare two specified bytes or two specified word

AAS ASCII adjust after subtraction.

DAS Decimal (BCD) adjust after subtraction.

Multiplication Instructions

MUL — Multiply unsigned byte by byte or unsigned word by word

IMUL — Multiply signed byte by byte or signed word by word

AAM — ASCII adjust after multiplication

Division Instructions

DIV — Divide unsigned word by byte or unsigned double word by word

IDIV — Divide signed word by byte or signed double word by word

AAD — ASCII adjust before division

CBW — Fill upper byte of word with copies of sign bit of lower byte

- CWD Fill upper word of double word with copies of sign bit of lower word
- **III. Logic and Bit Manipulation Instructions (AND, OR, XOR)Logic instructions:** The logical instructions perform basic AND, OR, XOR, and NOT logical operations on byte, word, and double word values. The bit and instructions test and modify individual bits in the bits in word and double word operands.

NOT — Invert each bit in a byte or word

AND — AND the content of a byte or a word with another byte or word

OR — OR the content of a byte or a word with another byte or word

XOR — Exclusive OR the content of a byte or a word with another byte or word

Shift Instructions

- SHL/SAL Shift bits of word or byte left, put zero(s) in LSB(s)
- **SHR** Shift bits of word or byte right, put zero(s) in MSB(s)
- SAR Shift bits of word or byte right, copy old MSB into new MSB

Rotate Instructions

- ROL Rotate bits of byte or word left, MSB to LSB and to CF
- ROR Rotate bits of byte or word right, LSB to MSB and to CF
- RCL Rotate bits of byte or word left, MSB to CF and CF to LSB
- RCR Rotate bits of byte or word right, LSB to CF and CF to MSB
- DAA Decimal (BCD) adjust after addition.
- SUB Subtract byte from byte or word from word.
- SBB Subtract byte and carry flag from byte word and carry flag from word.
- **DEC** Decrement specified byte or specified word by l.
- NEG Negate invert each bit of a specified byte or word and add 1 (form 2's complement).
- CMP Compare two specified bytes or two specified word
- AAS ASCII adjust after subtraction.
- DAS Decimal (BCD) adjust after subtraction.
- IV. String Instructions A string is a series of bytes or a series of words in sequential memory locations. A string often consists of ASCII character codes. In the list, a "/" is used to separate different mnemonics for the same instruction. Use the mnemonic which most clearly describes the function of the instruction in a specific application. A "B" In a mnemonic is used to specifically indicate that a string of bytes is to be acted upon. A "W" In the mnemonic is used to indicate that a string of words Is to be acted upon.

REP — An instruction prefix. Repeat following instruction until CX = 0

REPE/REPZ — An instruction prefix. Repeat instruction until CX = 0 or zero Flag ZF!=1

REPNE/REPNZ — An instruction prefix. Repeat until CX = 0 or ZF = 1

MOVS/MOVSB/MOVSW — Move byte or word from one string to another

COMPS/COMPSB/COMPSW — Compare two string bytes or two string words

INS/INSB/INSW (80186/80188) — Input string byte or word from port

OUTS/OUTSB/OUTSW (80186/80188) - output string byte or word to port

SCAS/SCASB/SCASW — Scan a string. Compare a string byte with a byte in AL or a string word with a word in AX

LODS/LODSB/LODSW — load string byte into AL or string word into AX

STOS/STOSB/STOSW — Store byte from AL or word from AX into string

V. Program Execution Transfer Instructions Instructions are used to tell the 8086 to start fetching instructions from some new address, rather than continuing in sequence.

Unconditional Transfer Instructions

- CALL Call a procedure (subprogram), save return address on stack
- **RET** Return from procedure to calling program
- JMP Go to specified address to get next instruction

Conditional Transfer Instructions

A "/" is used to separate two **mnemonics** which represent the same instruction. Use the mnemonic which most dearly describes the decision condition in a specific program. These instructions are often used after a compare instruction. The terms below and above refer to unsigned binary numbers. Above means larger in magnitude. The terms greater than or less than refer to signed binary numbers. Greater than means more positive.

JA/JNBE — Jump if above/Jump if not below or equal

JAE/JNB — Jump if above or equal/Jump if not below

JB/JNAE — Jump if below/Jump if not above or equal

JBE/JNA — Jump if below or equal/Jump if not above

JC — Jump if carry flag CF 1

JE/JZ — Jump if equal/Jump if zero flag ZF = 1

JG/JNLE — Jump if greater/Jump if not less than or equal

JGE/JNL — Jump if greater than or equal Jump if not less than

JL/JNGE — Jump if less than/Jump if not greater than or equal

JLE/JNG — Jump if less than or equal/Jump if not greater than

JNC — Jump if no carry (CF = 0)

JNE/JNZ — Jump if not equal/lump if not ' zero (ZF = 0)

JNO — Jump if no overflow (overflow flag OF = 0)

JNP/JPO — Jump if not parity/Jump if parity odd (PF = 0)

JNS — Jump if not sign (sign flag SF=0)

JO — Jump if overflow flag OF=1

JP/JPE — Jump if parity/Jump if parity even (PF =1)

JS — Jump if sign (SF = 1)

Iteration Control Instructions

These instructions can be used to execute a series of instructions some number of times. Here mnemonics separated by a "/" represent the same instruction. Use the one that best fits the specific application.

LOOP — Loop through a sequence of instructions until CX= 0

LOOPE/LOOPZ — Loop through a sequence instructions while ZF= 1 and CX != 0

LOOPNE/LOOPNZ — Loop through a sequence instructions while ZF=0 and CX != 0

JCXZ — Jump to specified address if CX=0

Interrupt Instructions

- INT- Interrupt program execution call service procedure
- **INTO** Interrupt program execution OF =1
- IRET Return from interrupt se procedure to main program

High-level Language Interface Instructions:

ENTER (80186/80188 only) — Enter procedure

LEAVE (80186/80188 only) — Leave procedure

BOUND (80186/80188 only) --- Check effective address within specified array bounds

VI. Processor Control Instructions: Executed to control processors operations

Flag set/clear Instructions:

STC — Set carry flag CF to 1

CLC — Clear carry flag CF to 0

CMC — Complement the state of the carry flag CF

STD — Set direction flag DF to 1 (decrement string pointers)

CLD — Clear direction flag DF to 0

STI — Set interrupt enable flag to 1 (enable INTR input)

CLI — Clear interrupt enable flag to 0 (disable INTR input)

Execution Control Instructions

HLT — Halt (do nothing) until interrupt or reset

WAIT — Wait (do nothing) until signal on the test pin is low

ESC — Escape to external coprocessor such as 8087 or 8089

LOCK — An instruction prefix. Prevents another processor from taking the bus while the adjacent instruction executes

NOP — No action except fetch and decode

11.3 TIMING CONTROL

Write Cycle Timing Diagram for Minimum Mode

- The working of the minimum mode configuration system can be better described in terms of the timing diagrams rather than qualitatively describing the operations.
- The opcode fetch and read cycles are similar. Hence the timing diagram can be categorized in two parts, the first is the timing diagram for read cycle and the second is the timing diagram for write cycle.
- The read cycle begins in T1 with the assertion of address latch enable (ALE) signal and also M / IO signal. During the negative going edge of this signal, the valid address is latched on the local bus.
- \bullet The BHE and A0 signals address low, high or both bytes. From T1 to T4 , the M/IO signal indicates a memory or I/O operation.

• At T2, the address is removed from the local bus and is sent to the output. The bus is then tristated.

The read (RD) control signal is also activated in T2.

• The read (RD) signal causes the address device to enable its data bus drivers. After RD goes low, the valid data is available on the data bus.



Fig. 11.1: Write Cycle diagram for Minimum Mode

- The addressed device will drive the READY line high. When the processor returns the read signal to high level, the addressed device will again tri-state its bus drivers.
- A write cycle also begins with the assertion of ALE and the emission of the address. The M/IO signal is again asserted to indicate a memory or I/O operation. In T2, after sending the address in T1, the processor sends the data to be written to the addressed location.
- The data remains on the bus until middle of T4 state. The WR becomes active at the beginning of T2 (unlike RD is somewhat delayed in T2 to provide time for floating).
- The BHE and A0 signals are used to select the proper byte or bytes of memory or I/O word to be read or write.
- The M/IO, RD and WR signals indicate the type of data transfer.
11.3.1 Bus Request and Bus Grant Timings in Minimum Mode System of 8086



Fig. 11.2: Bus Request and Bus Grant Timings in Minimum mode system

Hold Response sequence: The HOLD pin is checked at leading edge of each clock pulse. If it is received active by the processor before T4 of the previous cycle or during T1 state of the current cycle, the CPU activates HLDA in the next clock cycle and for succeeding bus cycles, the bus will be given to another requesting master.

The control of the bus is not regained by the processor until the requesting master does not drop the HOLD pin low. When the request is dropped by the requesting master, the HLDA is dropped by the processor at the trailing edge of the next clock.

Memory Read Timing Diagram in Maximum Mode of 8086



Fig. 11.3: Memory Read Time in Maximum Mode



11.3.2 Memory Write Timing in Maximum mode of 8086

Fig. 11.4: Memory Write Time in Maximum Mode

11.3.3. RQ/GT Timings in Maximum Mode



Fig. 11.5: RQ/GT Timings in Maximum Mode

The request/grant response sequence contains a series of three pulses. The request/grant pins are checked at each rising pulse of clock input.

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- When a request is detected and if the condition for HOLD request is satisfied, the processor issues a grant pulse over the RQ/GT pin immediately during T4 (current) or T1 (next) state.
- When the requesting master receives this pulse, it accepts the control of the bus, it sends a release pulse to the processor using RQ/GT pin.

11.4 INSTRCTION FORMATS

normally defines the location that contains the operand. The Instruction formats vary between microprocessors and minicomputers and mainframe computers. As the machine instructions are generally longer in larger computers with their larger memory words, the instruction format or how the instruction is translated differs. Each instruction is composed of fields. The lengths of instructions and the lengths and positions of the fields differ depending on the instruction and the computer. An operation (function) code is part of all instructions. How the remainder of the instruction is translated and the names assigned to the parts vary. Let's take a look at two examples of computer instruction formats, one for a microcomputer and one for a mainframe. We begin with the op (function) code, which is common to both; only the length differs. A typical machine instruction begins with the specification of an operation to be performed, the **operation (op) code**. The op code tells the computer/processor what basic operation to perform. The op code, a part of every instruction, is usually located at the beginning of each instruction format. Following the op code is information, if needed, to define the location of the data or the operand on which the operation is to be performed. This location in memory, called the operand address, at the start of the operation (the source), or that will contain the modified operand upon completion of the operation (the destination). The remainder of the instruction and how it is structured differs from one computer or computer type to another. The designators in each field and the positions of the fields within the instruction determine how the instruction will affect the operand, registers, memory, and general flow of data in and out of the computer.

11.4.1 General Instruction Format

Opdcode – Field Address – Field

- **Op-field:** specifies the operation to be performed;
- Address-field: provides operands or the CPU register/MM addresses of the operands.

Example:

x = (A + B) * (C + D)

whereA, B, C, D and X are five main memory locations representing five variables;

3-address format:

Assume variables A, B, C, D, and X are stored in MM locations labeled by their names.

ADD	R1	А	В	$\# R1 \leftarrow [A] + [B]$	
ADD	R2	С	D	$\# R2 \leftarrow [C] + [D]$	
MUI	X	R1	R2	# X←[R1] [R2]	

Note: here we assume an instruction *OP dst srcl src2* means:

 $dst \leftarrow [srcl] * [src2]$

where src1 and src2 are the *source operand*, dst is the *destination operand*, and * represents the operation specified in Op-code field OP.

MOV	R1	А	#	$R1 \leftarrow [A]$
ADD	R1	В	#	$R1 \leftarrow [B] + [R1]$
MOV	R2	С	#	R2← [C]
ADD	R2	D	#	$R2 \leftarrow [D] + [R2]$
MUL	R2	R1	#	$R2 \leftarrow [R1] [R2]$
MOV	Х	R2	#	$X \leftarrow [R2]$

• 2-Address Format:

• Note: here we assume an instruction *OP dst src* means:

- $dst \leftarrow [dst] * [stc]$
- where src is the *source operand*, dst is the *destination operand*, and * represents the operation specified in Op-code field OP.
- 1-Address Format:

Always use an implied accumulator (AC).

MOV	R1	#	$R1 \leftarrow [A]$
LOAD	А	#	$AC \leftarrow [A]$
ADD	В	#	$AC \leftarrow [AC] + [B]$
STORE	R	#	$R \leftarrow [AC]$
LOAD	С	#	$AC \leftarrow [C]$
ADD	D	#	$AC \leftarrow [AC] + [D]$
MUL	R	#	$AC \leftarrow [AC] \times [R]$
STORE	Х	#	$X \leftarrow [AC]$

• 0-Address Format:

used in stack-organized computer.

First, the given notation of the operation is converted into "reversed Polish notation (RPN)" :

 $(A + B) \times (C + D) \Rightarrow AB + CD + \times$ then execute this program:

- PUSH A PUSH B
- ADD
- PUSH C
- PUSH D
- ADD
- MUL
- POP X



Fig. 11.6: PUSH and POP Operation

- Stack A last-in, first-out (LIFO) data structure.
- Queue A first-in, first-out (FIFO) data structure.



Fig. 11.7: Two Operations-LIFO, FIFO

11.4.2 Three Instruction Formats

• R-type (register type)



Fig. 11.8: R-Type Instruction Format

where

- op: operation of the instruction;
- rs: the first register for source operand;
- rt: the second register for source operand;
- rd: the register for destination operand;
- shamt: shift amount;
- funct: function, selecting the variant of the operations in op field.

Format of Arithmetic Instruction

2 bits	6 bits	4 bits	4 bits	4 bits	12 bits
00	OPCODE	S-reg	S-reg	D-reg	000

Fig. 11.9: Format of Arithmetic Instruction

The first two bits are always 00, indicating that the instruction is an Arithmetic or Register transfer type of instruction. S-reg is the source register. D-reg is the destination register. The last 12 bits are always 0, as they are not used.

Note:

- The destination register is specified first (on the left) in assembly form, but last (on the right) in the actual binary form.
- In all R-type instructions (arithmetic, logical, shift, etc.), the operations are specified by the function field (6 least significant bits) in the binary instruction, with the opcode field (6 most significant bits) equal to zero.

Operation funct	Sll 0	Srl 2	jr 8	mfhi 16	mflo 18	mult 24	multu 25	div 26	divu 27
Operation	add	addu	sub	subu	and	or	slt	slti	
funct	32	33	34	35	36	37	42	43	

Examples:

Addition

add \$t0, \$s1, \$s2

0 17 18 8 0 32

000000 10001 10010 01000 00000 100000

• Subtraction



0 17 18 8 0 34

• Set-if-less-than





• I-type

I-type	op	rs	rt	address/immediate		
	Transfer, branch, immediate.					
Field size	6 bits	5bits	5bits	16 bits		

Fig. 11.10: I-Type Instruction Format

where

op: operation of the instruction;

rs: source register;

rt: destination register;

address: 16-bit field for the offset, or an immediate operand.

Conditional Branch and Immediate format

2 buts	6 buts	4 bits	4 buts	16 buts
01	OPCODE	B-reg	D-reg	Address

Fig. 11.11: Format of Conditional & Immediate

The first two bits are always 01, indicating that the instruction is a Conditional Branch and Immediate type of instruction. B-reg is the base register. D-reg is the destination register. The last 16 bits may be an address or an immediate data.

- When the last 16 bits contain data, the D-reg is always 0000.
- The Address may at times be treated as data, which is direct addressing.
- An indirect Address is calculated as :

Effective Address = Content (B-reg) + Address

• Conditional Branch checks for B and D reg to cause a branch, to a specified Address, or not

Examples:

load word

1w \$t0, Astart (\$s3)

 $1200_{10} = 0000010010110000_2$ assuming Astart is

35 19 8 1200

100011 10011 01000 0000 0100 1011 0000

• Save word

1w \$t0, Astart (\$s3)

43 19 8 1200

101011 10011 01000 0000 0100 1011 0000

• Brance-if-equal

beq \$s1, \$s2, 100

4 17 18 100

• Brance-if-not-equal

bne \$s1, \$s2, 100

5 17 18 100

• Add (immediate)

addi \$t1, \$s1, 100

8 17 9 100

• Set-if-less-then (immediate)

slti \$t1, \$s1, 100

10 17 9 100

• J-type



Fig. 11.12: J-Type instruction Format

Unconditional Jump Format

2 bits	6 bits	24 bits
10	OPCODE	Address

The first two bits are always 10, indicating that the instruction is an Unconditional Jump type of instruction, with a jump to the specified Address.

Examples:

• Jump

 $J\,10000$

000010 100000

Jump-and-link

jal 10000

000011 10000

11.5 GLOSSARY

Instruction Code: is collection of bits that instruct the computer to perform a specific operation.

Operation is a binary code that instructs the computer to perform a specific operation

Instruction Set: is the instruction code format of for specific computer

Data Transfer Instructions: The data transfer instructions move data between memory and the general-purpose and segment registers

Arithmetic Instructions: perform basic binary integer computations on byte, word, and double word integers located in memory and/or the general purpose registers

Logic and Bit Manipulation Instructions (AND, OR, XOR) Logic Instructions: The logical instructions perform basic AND, OR, XOR, and NOT logical operations on byte, word, and double word values. The bit and instructions test and modify individual bits in the bits in word and double word operands.

String Instructions: Works on series of Bytes or words

Program Execution Transfer Instructions: are used to start fetching instructions from some new address, rather than continuing in sequence

Iteration Control Instructions: can be used to execute a series of instructions some number of times.

Processor Control Instructions: Executed to control processors operations

Operation (op) code. tells the computer/processor what basic operation to perform

Address-field: provides operands or the CPU register/MM addresses of the operands.

Stack A last-in, first-out (LIFO) data structure.

Queue A first-in, first-out (FIFO) data structure.

11.6 REVIEW QUESTIONS

- Q.1 Define & differentiate between Instruction, Instruction Code, Instruction Format, & Instruction Set
- Q.2 Write the various types of Data Transfer Instructions.
- Q.3 How arithmetic Instruction works on Data? Write any 5 Instructions with description of each.
- Q.4 How the logical and Bit Instructions works discuss all logical and bit Instructions with Syntax.
- Q.5 What is String Instructions? Write any 4 String instructions.
- Q.6 What are Three, Two One and Zero Address Format? How each are differ from other?

Differentiate Between

- (i) PUSH and PUSHA
- (ii) POP and POPA
- (iii) ADD and ADC
- (iv) DIV and IDIV
- (v) Shift and Rotate
- (vi) CALL and JMP
- (vii) LOOP and LOOPE
- (viii) R-Type, J-Type and I-Type Instruction Format
- (ix) LIFO AND FIFO

Write Short Note On

- (i) Timing and Control Diagram
- (ii) Format of Arithmetic Instructions
- (iii) Conditional Branch and immediate Format
- (iv) Interrupt Instructions
- (v) High-level language interface instructions.

Chapter 12

Interrupt and Stack Organisation

12.0 OBJECTIVES

- · Concept of Interrupt
- Interrupt Types
 - Synchronous
 - Asynchronous
- Maskable Interrupt
- Non-maskable Interrupt (NMI)
- Inter-processor Interrupt (IPI)
- Software Interrupt
- Spurious Interrupt
- Interrupt Latency
- Interrupt Response Time
- Stack Organization
 - Register Stack
 - Memory Stack
- Reverse Polish Notation

12.1 INTRODUCTION

What is an Interrupt?

It is usually necessary for the processor to be capable of switching between a numbers of distinct processes upon receipt of appropriate signals. Each process generates its own signal demanding attention. These signals are known as *interrupt requests* since they each ask the processor to *interrupt* the process currently running. Therefore In computing, an **interrupt** is an asynchronous signal indicating the need for attention or a synchronous event in software indicating the need for a change in execution.

Or

An *interrupt* (also known as an *exception* or *trap*) is an event that causes the CPU to stop executing the current program and start executing a special piece of code called an *interrupt handler* or *interrupt service routine* (ISR). The ISR typically does some work, and then resumes the interrupted program.

• Interrupt are Similar to a procedure call:

- 1. can occur between any two instructions of the program
- 2. is transparent to the running program (usually)
- 3. is typically not explicitly requested by the program
- 4. calls a routine at an address determined by the type of interrupt, not by the program
- 5. atomically changes some processor mode bits in the Machine Status Register (MSR)

12.2 INTERRUPT TYPES

There are TWO Types of Interrupt based on relation with instruction in Microprocessors

1. Synchronous (instruction-related)

- illegal instruction
- privileged instruction
- bus error ("machine check")
- divide by 0 (on most processors),
- floating-point errors
- virtual memory page fault
- system call (into operating system)

2. Asynchronous: (not instruction-related)

- external hardware device
- timer expiration
- reset
- power failure
- on-chip debugging (on 823)
- A *hardware Interrupt* causes the processor to save its state of execution and begin execution of an interrupt handler.
- **Software** interrupts are usually implemented as instructions in the instruction set, which cause a context switch to an interrupt handler similar to a hardware interrupt.
- Interrupts are a commonly used technique for computer multitasking, especially in real-time computing. Such a system is said to be interrupt-driven.
- An act of *interrupting* is referred to as an Interrupt Request (IRQ).

Hardware Interrupts were introduced as a way to avoid wasting the processor's valuable time in polling loops, waiting for external events. They may be implemented in hardware as a distinct system with control lines, or they may be integrated into the memory subsystem.

Interrupts can be categorized into:

- (i) Maskable interrupt
- (ii) Non-maskable interrupt (NMI)
- (iii) Inter-processor interrupt (IPI)
- (iv) Software interrupt, and
- (v) Spurious interrupt.

12.2.1 Maskable Interrupt(MI)

is a hardware interrupt that may be ignored by setting a bit in an interrupt mask register's (IMR) bitmask. The processor can inhibit certain types of interrupts by use of a special interrupt mask bit. This mask bit is part of the flags/condition code register, or a special interrupt register. In the 8086 microprocessor if this bit is clear, and an interrupt request occurs on the Interrupt Request input, it is ignored.

12.2.2 Non-maskable Interrupt

(NMI) is a hardware interrupt that lacks an associated bit-mask, so that it can never be ignored. NMIs are often used for timers, especially watchdog timers. These are associated with high priority tasks which cannot be ignored (like memory parity or bus faults). In general, most processors support the Non-Maskable Interrupt (NMI). This interrupt has absolute priority, and when it occurs, the processor will finish the current memory cycle, then branch to a special routine written to handle the interrupt request.

12.2.3 Inter-Processor Interrupt

(IPI) is a special case of interrupt that is generated by one processor to interrupt another processor in a multiprocessor system.

12.2.4 Software Interrupt

is an interrupt generated within a processor by executing an instruction. Software interrupts are often used to implement system calls because they implement a subroutine call with a CPU ring level change.

12.2.5 Spurious Interrupt

is a hardware interrupt that is unwanted. They are typically generated by system conditions such as electrical interference on an interrupt line or through incorrectly designed hardware.

12.3 TYPES OF INTERRUPTS

12.3.1 Level-triggered

A level-triggered interrupt is a class of interrupts where the presence of an un-serviced interrupt is indicated by a particular state, high level or low level, of the interrupt request line. A device wishing to signal an interrupt drives line to its active level, and then holds it at that level until serviced. It ceases asserting the line when the CPU commands it to or otherwise handles the condition that caused it to signal the interrupt.

12.3.2 Edge-triggered

An **edge-triggered interrupt** is a class of interrupts that are signalled by a level transition on the interrupt line, either a falling edge (high to low) or a rising edge (low to high). A device wishing to signal an interrupt drives a pulse onto the line and then releases the line to its inactive state. If the pulse is too short to be detected by polled I/O then special hardware may be required to detect the edge.

Multiple devices may share an **edge-triggered interrupt line** if they are designed to. The interrupt line must have a pull-down or pull-up resistor so that when not actively driven it settles to one particular state. Devices signal an interrupt by briefly driving the line to its non-default state, and let the line float (do not actively drive it) when not signalling an interrupt. This type of connection is also referred to as open collector. The line then carries all the pulses generated by all the devices. (This is analogous to the pull cord on some buses and trolleys that any passenger can pull to signal the driver that they are requesting a stop.) However, interrupt pulses from different devices may merge if they occur close in time. To avoid losing interrupts the CPU must trigger on the trailing edge of the pulse (e.g. the rising edge if the line is pulled up and driven low). After detecting an interrupt the CPU must check all the devices for service requirements.

Edge-triggered interrupts do not suffer the problems that **level-triggered interrupts** have with sharing. Service of a low-priority device can be postponed arbitrarily, and interrupts will continue to be received from the high-priority devices that are being serviced. If there is a device that the CPU does not know how to service, it may cause a spurious interrupt, or even periodic spurious interrupts, but it does not interfere with the interrupt signalling of the other devices. However, it is fairly easy for an edge triggered interrupt to be missed - for example if interrupts have to be masked for a period - and unless there is some type of hardware latch that records the event it is impossible to recover. Such problems caused many "lockups" in early computer hardware because the processor did not know it was expected to do something. More modern hardware often has one or more interrupt status registers that latch the interrupt requests; well written edge-driven interrupt software often checks such registers to ensure events are not missed.

The elderly **Industry Standard Architecture (ISA)** bus uses edge-triggered interrupts, but does not mandate that devices be able to share them. The parallel port also uses edge-triggered interrupts. Many older devices assume that they have exclusive use of their interrupt line, making it electrically unsafe to share them. However, ISA motherboards include pull-up resistors on the IRQ lines, so wellbehaved devices share ISA interrupts just fine.

12.3.3 Hybrid Interrupt

Some systems use a hybrid of level-triggered and edge-triggered signalling. The hardware not only looks for an edge, but it also verifies that the interrupt signal stays active for a certain period of time.

A common use of a hybrid interrupt is for the NMI (non-maskable interrupt) input. Because NMIs generally signal major – or even catastrophic – system events, a good implementation of this signal tries to ensure that the interrupt is valid by verifying that it remains active for a period of time. This 2-step approach helps to eliminate false interrupts from affecting the system.

12.3.4 Message-signaled Interrupt

A **message-signalled interrupt** does not use a physical interrupt line. Instead, a device signals its request for service by sending a short message over some communications medium, typically a computer. The message might be of a type reserved for interrupts, or it might be of some pre-existing type such as a memory write.

Message-signalled interrupts behave very much like edge-triggered interrupts, in that the interrupt is a momentary signal rather than a continuous condition. Interrupt-handling software treats the two in

much the same manner. Typically, multiple pending message-signalled interrupts with the same message (the same virtual interrupt line) are allowed to merge, just as closely-spaced edge-triggered interrupts can merge.

Message-signalled interrupt vectors can be shared, to the extent that the underlying communication medium can be shared. No additional effort is required.

Because the identity of the interrupt is indicated by a pattern of data bits, not requiring a separate physical conductor, many more distinct interrupts can be efficiently handled. This reduces the need for sharing. Interrupt messages can also be passed over a serial bus, not requiring any additional lines.

12.3.5 Doorbell

In a push button analogy applied to computer systems, the term **doorbell or doorbell interrupt** is often used to describe a mechanism whereby a software system can signal or notify a hardware device that there is some work to be done. Typically, the software system will place data in some well known and mutually agreed upon memory location(s), and "ring the doorbell" by writing to a different memory location. This different memory location is often called the doorbell region, and there may even be multiple doorbells serving different purposes in this region. It's this act of writing to the doorbell region of memory that "rings the bell" and notifies the hardware device that the data is ready and waiting. The hardware device would now know that the data is valid and can be acted upon. It would typically write the data to a hard disk drive, or send it over a network, or encrypt it, etc.

12.4 ITERURRUPT IN 8086

There are two main types of interrupt in the 8086 microprocessor, internal and external hardware interrupts. Hardware interrupts occur when a peripheral device asserts an interrupt input pin of the microprocessor. Whereas internal interrupts are initiated by the state of the CPU (e.g. divide by zero error) or by an instruction.

Provided the interrupt is permitted, it will be acknowledged by the processor at the end of the current memory cycle. The processor then services the interrupt by branching to a special service routine written to handle that particular interrupt. Upon servicing the device, the processor is then instructed to continue with what is was doing previously by use of the "return from interrupt" instruction.

The status of the programme being executed must first be saved. The processors registers will be saved on the stack, or, at very least, the programme counter will be saved. Preserving those registers which are not saved will be the responsibility of the interrupt service routine. Once the programme counter has been saved, the processor will branch to the address of the service routine.

12.4.1 Advantages of Interrupts

Interrupts are used to ensure adequate service response times by the processing. Sometimes, with software polling routines, service times by the processor cannot be guaranteed, and data may be lost. The use of interrupts guarantees that the processor will service the request within a specified time period, reducing the likelihood of lost data.

12.4.2Interrupt Latency

The time interval from when the interrupt is first asserted to the time the CPU recognises it. This will depend much upon whether interrupts are disabled, prioritized and what the processor is currently executing. At times, a processor might ignore requests whilst executing some indivisible instruction stream (read-write-modify cycle). The figure that matters most is the longest possible interrupt latency time.

12.4.3 Interrupt Response Time

The time interval between the CPU recognising the interrupt to the time when the first instruction of the interrupt service routine is executed. This is determined by the processor architecture and clock speed.

The Operation of an Interrupt sequence on the 8086 Microprocessor:

- 1. External interface sends an interrupt signal, to the Interrupt Request (INTR) pin, or an internal interrupt occurs.
- 2. The CPU finishes the present instruction (for a hardware interrupt) and sends Interrupt Acknowledge (INTA) to hardware interface.
- 3. The interrupt type N is sent to the Central Processor Unit (CPU) via the Data bus from the hardware interface.
- 4. The contents of the flag registers are pushed onto the stack.
- 5. Both the interrupt (IF) and (TF) flags are cleared. This disables the INTR pin and the trap or single-step feature.
- 6. The contents of the code segment register (CS) are pushed onto the Stack.
- 7. The contents of the instruction pointer (IP) are pushed onto the Stack.
- The interrupt vector contents are fetched, from (4 x N) and then placed into the IP and from (4 x N +2) into the CS so that the next instruction executes at the interrupt service procedure addressed by the interrupt vector.
- 9. While returning from the interrupt-service routine by the Interrupt Return (IRET) instruction, the IP, CS and Flag registers are popped from the Stack and return to their state prior to the interrupt

12.5 STACK ORGANIZATION

The CPU of most computers comprises of a **stack or last-in-first-out (LIFO)** list where in information is stored in such a manner that the item stored last is the first to be retrieved. The operation of a stack can be compared to a stack of trays. The last tray placed on top of the stack is the first to be taken off.

The stack in digital computers is essentially a memory unit with an address register that can count only (after an initial value is loaded into it). A Stack Pointer (SP) is the register where the address for the stack is held because its value always points at the top item in the stack. The physical registers of a stack are always available for reading or writing unlike a stack of trays where the tray itself may be taken out or inserted because it is the content of the word that is inserted or deleted.

A stack has only two operations i.e. the insertion and deletion of items. The operation insertion is called push (or push-down) because it can be thought of as the result of pushing a new item on top. The

deletion operation is called pop (or pop-up) because it can be thought of as the result of removing one item so that the stack pops up. In actual, nothing is exactly pushed or popped in a computer stack. These operations are simulated by incrementing or decrementing the stack pointer register.

12.5.1 Register Stack

There are two ways to place a stack. Either it can be placed in a portion of a large memory or it can be organized as a collection of a finite number of memory words or registers. The organization of a 64-word register stack is exhibited. A binary number whose value is equal to the address of the word that is currently on top of the stack is contained by the stack pointer register. Three items are placed in the stack - A, B and C in that order. Item C is on top of the stack so that the content of SP is now 3. To remove the top item, the stack is popped by reading the memory word at address 3 and decrementing the content of SP. Item B is now on top of the stack since SP holds address 2. To insert a new item, the stack is pushed by incrementing SP and writing a word in the next-higher location in the stack. Note that item C has been read out but not physically removed.

This does not matter because when the stack is pushed, a new item is written in its place.

In a 64-word stack, the stack pointer contains 6 bits because $2^6 = 64$. Since SP has only six bits, it cannot exceed a number greater than 63 (111111 in binary). When 63 is incremented by l, the result is 0 since 111111 + 1 = 1000000 in binary, but SP can accommodate only the six least significant bits. Similarly, when 000000 is decremented by 1, the result is 111111. The 1-bit register FULL is set to 1 when the stack is full, and the one-bit register EMTY is set to 1 when the stack is empty of items.

DR is the data register that holds the binary data to be written into or read out of the stack. Initially, SP is cleared to 0, EMTY is set to 1, and FULL is cleared to 0, so that SP points to the word at address 0 and the stack is marked empty and not full. If the stack is not full (if FULL = 0), a new item is inserted with a push operation. The push operation is implemented with the following sequence of microoperations:

 $SP \leftarrow SP + 1$ Increment stack pointer

 $M[SP] \leftarrow DR$ Write item on top of the stack

If (SP = 0) then (FULL \leftarrow 1) Check if stack is full

The stack pointer is incremented so that it points to the address of the next-higher word. The word from DR is inserted into the top of the stack by the memory write operation. The M[SP] denotes the memory word specified by the address presently available in SP whereas the SP holds the address the top of the stack. The storage of the first item is done at address 1 whereas as the last item is store at address 0. If SP reaches 0, the stack is full of items, so FULL is set to 1. This condition is reached if the top item prior to the last push was in location 63 and after incrementing SP, the last item is stored in location 0. Once an item is stored in location 0, there are no more empty registers in the stack. If an item is written in the stack, obviously the stack cannot be empty, so EMTY is cleared to 0.

A new item is deleted from the stack if the stack is not empty (if EMTY <> 0). The pop operation consists of the following sequence of micro-operations:

 $DR \leftarrow M[SP]$ Read item from the top of stack

 $SP \leftarrow SP - 1$ Decrement stack pointer

If (SP == 0) then (FULL \leftarrow 1) Check if stack is empty

EMTY $\leftarrow 0$ Mark the stack not full

DR. reads the top item from the stack. Then the stack pointer is decremented. If its value attains zero, the stack is empty, so EMTY is set to 1. This condition is reached if the item read was in location 1. Once this item is read out, SP is decremented and it attain reaches the value 0, which is the initial value of SP. Note that if a pop operation reads the item from location 0 and then SP is decremented, SP changes to 111111, which is equivalent to decimal 63. In this configuration, the word in address 0 receives the last item in the stack. Note also that an erroneous operation will result if the stack is pushed when FULL = 1 or popped when EMPTY = 1.

12.5.2 Memory Stack

As shown in Fig. 12.1, stack can exist as a stand-alone unit or can be executed in a random-access memory attached to a CPU. The implementation of a stack in the CPU is done by assigning a portion of memory. A portion of memory is assigned to a stack operation and a processor register is used as a stack pointer to execute stack in the CPU.

The address of the next instruction in the program is located by the program counter PC while an array of data is pointed by address register AR. The top of the stack is located by the stack pointer SP. The three registers are connected to a common address bus, which connects the three registers and either one can provide an address for memory. PC is used during the fetch phase to read an instruction. AR is used during the execute phase to read an operand. SP is used to push or pop items into or from the stack.



Fig. 12.1: Computer Memory with program, data, and slack segments

Fig 12.0 displays the initial value of SP at 4001 and the growing of stack with decreasing addresses. Thus the first item stored in the stack is at address 4000, the second item is stored at address 3999, and the last address that can be used for the stack is 3000. No checks are provided for checking stack limits.

We assume that the items in the stack communicate with a data register DR. A new item is inserted with the push operation as follows:

 $SP \leftarrow SP - 1$

 $M[SP] \leftarrow DR$

The stack pointer is decremented so that it points at the address of the next word. A memory write operation inserts the word form DR into the top of the stack. A new item is deleted with a pop operation as follows:

 $DR \leftarrow M[SP]$

 $SP \leftarrow SP + 1$

The top item is read from the stack into DR. The stack pointer is then incremented to point at the next item in the stack.

Most computers are not equipped with hardware to check for stack overflow (full stack) or underflow (empty stack). The stack limits can be checked by using two processor registers: one to hold the upper limit (3000 in this case), and the other to hold the lower limit (40001 in this case). After a push operation, SP is compared with the upper-limit register and after a pop operation, SP is compared with the lower-limit register.

12.5.3 Reverse Polish Notation

Reverse Polish Notation is a way of expressing arithmetic expressions that avoids the use of brackets to define priorities for evaluation of operators. In ordinary notation, one might write (3 + 5) * (7 - 2) and the brackets tell us that we have to add 3 to 5, then subtract 2 from 7, and multiply the two results together. In RPN, the numbers and operators are listed one after another, and an operator always acts on the most recent numbers in the list.

The numbers can be thought of as forming a stack, like a pile of plates. The most recent number goes on the top of the stack.

An operator takes the appropriate number of arguments from the top of the stack and replaces them by the result of the operation. In this notation the above expression would be

3 5 + 7 2 - *

Reading from left to right, this is interpreted as follows:

- Push 3 onto the stack.
- Push 5 onto the stack. The stack now contains (3, 5).
- Apply the + operation: take the top two numbers off the stack, add them together, and put the result back on the stack. The stack now contains just the number 8.
- Push 7 onto the stack.
- Push 2 onto the stack. It now contains (8, 7, 2).
- Apply the operation: take the top two numbers off the stack, subtract the top one from the one below, and put the result back on the stack. The stack now contains (8, 5).

• Apply the * operation: take the top two numbers off the stack, multiply them together, and put the result back on the stack. The stack now contains just the number 40.

Polish Notation was devised by the Polish philosopher and mathematician Jan Lucasiewicz (1878-1956) for use in symbolic logic. In his notation, the operators preceded their arguments, so that the expression above would be written as

* + 3 5 - 7 2

The 'reversed' form has however been found more convenient from a computational point of view.

12.6 GLOSSARY

Interrupt: is an event that causes the CPU to stop executing the current program and start executing a special piece of code called an interrupt handler.

Synchronous Interrupt: related to Instructions

Asynchronous Interrupt: Not Related to Instructions

ISR: Interrupt Service Routine

IMR: Interrupt Mask Register

Maskable Interrupt (MI): is a hardware interrupt that may be ignored by setting a bit in an interrupt mask register's (IMR) bit-mask.

Non-maskable interrupt (NMI): is a hardware interrupt that lacks an associated bit-mask, so that it can never be ignored

Inter-Processor Interrupt (IPI): is a special case of interrupt that is generated by one processor to interrupt another processor in a multiprocessor system.

Software interrupt: is an interrupt generated within a processor by executing an instruction

Spurious interrupt: is a hardware interrupt that is unwanted.

Level-Triggered Interrupt: is a class of interrupts where the presence of an un-serviced interrupt is indicated by a particular state, high level or low level, of the interrupt request line

Edge-Triggered Interrupt: is a class of interrupts that are signalled by a level transition on the interrupt line, either a falling edge (high to low) or a rising edge (low to high)

Hybrid Interrupt: Hybrid of level-triggered and edge-triggered signalling

Message-Signalled Interrupt: A device signals its request for service by sending a short message over some communications medium.

Doorbell Interrupt : is used to describe a mechanism whereby a software system can signal or notify a hardware device that there is some work to be done.

Interrupt Latency: The time interval from when the interrupt is first asserted to the time the CPU recognises

Interrupt Response Time: The time interval between the CPU recognising the interrupt to the time when the first instruction of the interrupt service routine is executed

Stack Organization: The CPU of most computers comprises of a stack or last-in-first-out (LIFO) list where in information is stored in such a manner that the item stored last is the first to be retrieved.

Register Stack: Stack is implemented in Register

Memory Stack: stack is implemented in some portion of memory

Reverse Polish Notation: is a way of expressing arithmetic expressions that avoids the use of brackets to define priorities for evaluation of operators

Address Sequencing: It is the procedure for ensuring that received address messages concerning a call attempt are processed in the correct order

12.7 REVIEW QUESTIONS

Q.1 What are Interrupts? How Interrupts is similar to Procedure?

- Q.2 Discuss the various categories of Interrupt.
- Q.3 What are various Types of Interrupt? Explain each in detail.
- Q.4 What do you understand with term of 'Stack Organisation' Explain?
- Q.5 Discuss the Register and memory Stack Organization.

Write the Differences Between

- (i) Synchronous Interrupt and Asynchronous Interrupt
- (ii) Software Interrupt and Hardware Interrupt
- (iii) Maskable Vs Non-Maskable Interrupt
- (iv) Interrupt Latency and Interrupt Response Time
- (v) Register stack Vs Memory Stack

Write Short Note on

- (i) Interrupt service Routine
- (ii) Inter Process Interrupt
- (iii) Spurious Interrupt
- (iv) Edge-Triggered Interrupt
- (v) Door Bell Interrupt
- (vi) Reverse Polish Notation
- (vi) Address Sequencing

Chapter 13

Memory System and Micro-Instruction Sequencer and Format

13.0 OBJECTIVES

- Memory System
 - Main Memory
 - Secondary Memory
- Memory Hierarchy
- Cache Memory
 - Direct Mapping
 - Two Way Associative Mapping
 - Associative Mapping
- Replacement Algorithm
 - LRU
 - FIFO
 - LFU
- Writing Strategies
 - Write Through
 - Copy Back
- Virtual Memory
- Page Table
- Demand Paging Address Translation
- Control Memory
- Micro-Program Sequencer
- Micro-Instruction Format
- Micro-Operation

- Computer Register
- RTL

13.1 INTRODUCTION

Basically there is TWO main Types of Memory in computer organization:

- Main Memory: It has following characteristic features
 - fast, random access,
 - expensive,
 - Located close (but not inside) the CPU.
 - Is used to store program and data which are currently manipulated by the CPU.
- · Secondary Memory: It has following characteristic features
 - slow,
 - cheap,
 - direct access,
 - Located remotely from the CPU.

13.2 PROBLEMS WITH THE MEMORY SYSTEM

What do we need

We need memory to fit very large programs and to work at a speed comparable to that of the microprocessors, but the Main problem is:

- microprocessors are working at a very high rate and they need large memories;
- memories are much slower than microprocessors;

Facts

- the larger a memory, the slower it is;
- the faster the memory, the greater the cost/bit.

A Solution

It is possible to build a composite memory system which combines a small, fast memory and a large slow main memory and which behaves (most of the time) like a large fast memory.

The two level principles above can be extended into a hierarchy of many levels including the secondary memory (disk store).

The effectiveness of such a memory hierarchy is based on property of programs called the **principle** of locality



Fig. 13.1: Memory Hierarchy

Some typical characteristics of memories in the Hierarchy:

- 1. Processor Registers:
 - 32 registers of 32 bits each = 128 bytes
 - access time = few nanoseconds
- 2. On-chip Cache Memory:
 - capacity = 8 to 32 Kbytes
 - access time = ~ 10 nanoseconds
- 3. Off-chip Cache Memory:
 - \cdot capacity = few hundred Kbytes
 - \cdot access time = tens of nanoseconds

4. Main Memory:

- capacity = tens of Mbytes
- access time = ~ 100 nanoseconds

5. Hard Disk:

- capacity = few Gbytes
- access time = tens of milliseconds

The key to the success of a memory hierarchy is if data and instructions can be distributed across the memory so that most of the time they are available, when needed, on the top levels of the hierarchy.

- The data which is held in the registers is under the direct control of the compiler or of the assembler programmer.
- The contents of the other levels of the hierarchy are managed automatically:
- migration of data/instructions to and from caches is performed under hardware control;
- migration between main memory and backup store is controlled by the operating system (with hardware support).

13.3 CACHE MEMORY

A cache memory is a small, very fast memory that retains copies of recently used information from main memory. It operates transparently to the programmer, automatically deciding which values to keep and which to overwrite.



Fig. 13.2: Cache Memory

- The processor operates at its high clock rate only when the memory items it requires are held in the cache.
- The overall system performance depends strongly on the proportion of the memory accesses which can be satisfied by the cache
 - An access to an item which is in the cache: hit
 - An access to an item which is not in the cache: miss.
 - The proportion of all memory accesses that are satisfied by the cache: hit rate
 - The proportion of all memory accesses that are not satisfied by the cache: miss rate
 - The miss rate of a well-designed cache: few %
 - Cache space (~KBytes) is much smaller than main memory (~MBytes);
 - Items have to be placed in the cache so that they are available there when (and possibly only when) they are needed.
- How can this work?

The answer is: locality

During execution of a program, memory references by the processor, for both instructions and data, tend to cluster: once an area of the program is entered, there are repeated references to a small set of instructions (loop, subroutine) and data (components of a data structure, local variables or parameters

on the stack).

Temporal locality (locality in time): If an item is referenced, it will tend to be referenced again soon.

Spacial locality (locality in space): If an item is referenced, items whose addresses are close by will tend to be referenced soon.

Problems concerning cache memories:

- How many caches?
- How to determine at a read if we have a miss or hit?
- If there is a miss and there is no place for a new slot in the cache which information should be replaced?
- How to preserve consistency between cache and main memory at write?

Separate Data and Instruction Caches

- The figure shows architecture with a unified instruction and data cache.
- It is common also to split the cache into one dedicated to instructions and one dedicated to data.

Advantages of unified caches:

- They are able to better balance the load between instruction and data fetches depending on the dynamics of the program execution;
- Design and implementation are cheaper.

Advantages of split caches (Harvard Architectures)

• Competition for the cache between instruction processing and execution units is eliminated Instruction fetch can proceed in parallel with memory access from the execution unit.



Fig. 13.3: unified instruction & Data Cache

13.4 CACHE ORGANIZATION

Example:

A cache of 64 Kbytes

- Data transfer between cache and main memory is in blocks of 4 bytes; we say the cache is organized in lines of 4 bytes;
- A main memory of 16 Mbytes; each byte is addressable by a 24-bit address $(2^{24}=16M)$
- the cache consists of 2¹⁴ (16K) lines the main memory consists of 2²² (4M) blocks

Questions:

- When we bring a block from main memory into the cache where (in which line) do we put it?
- · When we look for the content of a certain memory address
- In which cache line do we look for it?
- · How do we know if we have found the right
- Information (hit) or not (miss)?

13.4.1 Direct Mapping



Fig. 13.4: Direct Mapping

If we had a miss, the block will be placed in the cache line which corresponds to the 14 bits field in the memory address of the respective block



memory block is mapped into a unique cache line, depending on the memory address of the respective block.

- A memory address is considered to be composed of Three fields:
- 1. The least significant bits (2 in our example)
 - Identify the byte within the block;
- The rest of the address (22 bits in our example)
 Identify the block in main memory; for the cache logic, this part is interpreted as two fields:
- 2a. the least significant bits (14 in our example) specify the cache line;
- 2b. the most significant bits (8 in our example) represent the tag, which is stored in the cache together with the line.
 - Tags are stored in the cache in order to distinguish among blocks which fit into the same cache line.

Advantages

- simple and cheap;
- the tag field is short; only those bits have to be stored which are not used to address the cache (compare with the following approaches);
- Access is very fast.

Disadvantage

• a given block fits into a fixed cache location a given cache line will be replaced whenever there is a reference to another memory block which fits to the same line, regardless what the status of the other cache lines is.

This can produce a low hit ratio, even if only a very small part of the cache is effectively used.

13.4.2 Two-way Set-associative Cache



Fig. 13.5: Two-Way Associative Mapping

If we had a miss, the block will be placed in one of the two cache lines belonging to that set which corresponds to the 13 bits field in the memory address. The replacement algorithm decides which line to use.

- A memory block is mapped into any of the lines of a set. The set is determined by the memory address, but the line inside the set can be any one.
- If a block has to be placed in the cache the particular line of the set will be determined according to a replacement algorithm.
- The memory address is interpreted as three fields by the cache logic, similar to direct mapping. However, a smaller number of bits (13 in our example) are used to identify the set of lines in the cache; correspondingly, the tag field will be larger (9 bits in our example).
 - Several tags (corresponding to all lines in the set) have to be checked in order to determine if we have a hit or miss. If we have a hit, the cache logic finally points to the actual line in the cache.
 - The number of lines in a set is determined by the designer;

- 2 lines/set: two-way set associative mapping
- 4 lines/set: four-way set associative mapping
- Set associative mapping keeps most of the advantages of direct mapping:
 - short tag field
 - fast access
 - relatively simple
- Set associative mapping tries to eliminate the main shortcoming of direct mapping; a certain flexibility is given concerning the line to be replaced when a new block is read into the cache.
- Cache hardware is more complex for set associative mapping than for direct mapping.
- In practice 2 and 4-way set associative mapping are used with very good results. Larger sets do not produce further significant performance improvement.
- if a set consists of a single line **Direct Mapping**;
- If there is one single set consisting of all lines > Associative Mapping.

13.4.3 Associtative Mapping



Fig. 13.6: Associative Mapping

If we had a miss, the block will be placed in one of the 2^{14} cache lines. The replacement algorithm decides which line to use.

- A memory block can be mapped to any cache line.
- If a block has to be placed in the cache the particular line will be determined according to a replacement algorithm.
- The memory address is interpreted as two fields by the cache logic. The lest significant bits (2 in our example) identify the byte within the block; All the rest of the address (22 bits in our example) is interpreted by the cache logic as a tag.
- All tags, corresponding to every line in the cache memory, have to be checked in order to determine if we have a hit or miss. If we have a hit, the cache logic finally points to the actual line in the cache. The cache line is retrieved based on a portion of its content (the tag field) rather than its address. Such a memory structure is called associative memory.

Advantages

• Associative mapping provides the highest flexibility concerning the line to be replaced when a new block is read into the cache.

Disadvantages

- Complex
- The tag field is long

• fast access can be achieved only using high Performance associative memories for the cache, which is difficult and expensive.

13.5 REPLACEMENT ALGORITHMS

When a new block is to be placed into the cache, the block stored in one of the cache lines has to be replaced.

- With direct mapping there is no choice.
- With associative or set-associative mapping a replacement algorithm is needed in order to determine which block to replace (and, implicitly, in which cache line to place the block)
- with set-associative mapping, the candidate lines are those in the selected set

· with associative mapping, all lines of the cache are potential candidates

Random Replacement: One of the candidate lines is selected randomly.

All the other policies are based on information concerning the usage history of the blocks in the cache.

Least Recently Used (LRU): The candidate line is selected which holds the block that has been in the cache the longest without being referenced.

First-in-first-out (FIFO): The candidate line is selected which holds the block that has been in the cache the longest.

Least Frequently Used (LFU): The candidate line is selected which holds the block that has got the fewest references.

• Replacement algorithms for cache management have to be implemented in hardware in order to be effective.

- LRU is the most efficient: relatively simple to implement and good results.
- FIFO is simple to implement.
- Random replacement is the simplest to implement and results are surprisingly good.

13.6 WRITE STRATEGIES

The problem

How to keep cache content and the content of main memory consistent without losing too much performance?

Problems arise when a write is issued to a memory address, and the content of the respective address is potentially changed.

13.6.1 Write-through

All write operations are passed to main memory; if the addressed location is currently hold in the cache, the cache is updated so that it is coherent with the main memory.

For writes, the processor always slows down to main memory speed.

13.6.2 Write-through with Buffered Write

The same as write-through, but instead of slowing the processor down by writing directly to main memory, the write address and data are stored in a high-speed write buffer; the write buffer transfers data to main memory while the processor continues its task.

- higher speed,
- more complex hardware

13.6.3 Copy-back

- Write operations update only the cache memory which is not kept coherent with main memory; cache lines have to remember if they have been updated; if such a line is replaced from the cache, its content has to be copied back to memory.
- good performance (usually several writes are performed on a cache line before it is replaced and has to be copied into main memory),
- complex hardware
- Cache coherence problems are very complex and difficult to solve in multiprocessor systems.

Some Cache Architectures

Intel 80486

- a single on-chip cache of 8 Kbytes
- line size: 16 bytes
- 4-way set associative organization

Pentium

- two on-chip caches, for data and instructions.
- each cache: 8 Kbytes
- line size: 32 bytes
- · 2-way set associative organization

13.7 WHAT IS VIRTUAL MEMORY

An imaginary memory area supported by some operating systems (for example, Windows but not DOS) in conjunction with the hardware. You can think of virtual memory as an alternate set of memory addresses. Programs use these *virtual addresses* rather than real addresses to store instructions and data. When the program is actually executed, the virtual addresses are converted into real memory addresses.

How it is Implemented

The address space needed and seen by programs is usually much larger than the available main memory.

Only one part of the program fits into main memory, the rest is stored on secondary memory (hard disk).

- In order to be executed or data to be accessed, a certain segment of the program has to be first loaded into main memory; in this case it has to replace another segment already in memory.
- Movement of programs and data, between main memory and secondary storage, is performed automatically by the operating system. These techniques are called virtual-memory techniques.
- The binary address issued by the processor is a virtual (logical) address; it considers a virtual address space, much larger than the physical one available in main memory.



Fig. 13.7: virtual Memory Organization

If a virtual address refers to a part of program or data that is currently in the physical memory (cache, main memory), then the appropriate location is accessed immediately using the respective physical address; if this is not the case, the respective program/data has to be transferred first from secondary memory.

• A special hardware unit, Memory Management Unit (MMU), translates virtual addresses into physical ones.

13.7.1 Virtual Memory Organization - Demand Paging

- The virtual programme space (instructions + data) is divided into equal, fixed-size chunks called pages.
- Physical main memory is organized as a sequence of frames; a page can be assigned to an available frame in order to be stored (page size = frame size).
- The page is the basic unit of information which is moved between main memory and disk by the virtual memory system.
- Common page sizes are: 2 16Kbytes.

Demand Paging

- The program consists of a large amount of pages which are stored on disk; at any one time, only a few pages have to be stored in main memory.
- The operating system is responsible for loading/ replacing pages so that the number of page faults is minimized.
- We have a page fault when the CPU refers to a location in a page which is not in main memory; this page has then to be loaded and, if there is no available frame, it has to replace a page which previously was in memory.



Fig. 13.8: Demand Paging

13.8 ADDRESS TRANSLATION

- Accessing a word in memory involves the translation of a virtual address into a physical one:
 - virtual address: page number + offset
 - physical address: frame number + offset
- Address translation is performed by the MMU using a page table.

Example:

- Virtual memory space: 2 Gbytes
 - (31 address bits; $2^{31} = 2$ G)
- Physical memory space: 16 Mbytes (2²⁴=16M)
- Page length: 2Kbytes $(2^{11} = 2K)$, therefore, Total number of pages: $2^{20} = 1M$ and Total number of frames: $2^{13} = 8K$



Fig. 13.9: Address Translation in Cache Memory

13.9 PAGE TABLE

Is the data structure used by a virtual memory system in a computer operating system to store the mapping between virtual addresses and physical addresses. Virtual addresses are those unique to the accessing process. Physical addresses are those unique to the hardware, i.e., RAM.

- The page table has one entry for each page of the virtual memory space.
- Each entry of the page table holds the address of the memory frame which stores the respective page, if that page is in main memory.

- Each entry of the page table also includes some control bits which describe the status of the page:
- Whether the page is actually loaded into main memory or not;
- If since the last loading the page has been modified;
- Information concerning the frequency of access, etc.

Problems

- The page table is very large (number of pages in virtual memory space is very large).
- Access to the page table has to be very fast, therefore the page table has to be stored in very fast memory, on chip.

A special cache is used for page table entries, called **translation lookaside buffer (TLB)**; it works in the same way as an ordinary memory cache and contains those page table entries which have been most recently used.

• The page table is often too large to be stored in main memory so that Virtual memory techniques are used to store the page table itself only part of the page table is stored in main memory at a given moment.

The page table itself is distributed along the memory hierarchy:

- TLB (cache)
- Main memory
- Disk





Fig. 13.10: Memory Reference with Virtual Memory and TLB
- Memory access is solved by hardware except the page fault sequence which is executed by the OS software.
- The hardware unit which is responsible for translation of a virtual address into a physical one is the **Memory Management Unit (MMU).**

13.10 PAGE REPLACEMENT

• When a new page is loaded into main memory and there is no free memory frame, an existing page has to be replaced.

The decision on which page to replace is based on the same speculations like those for replacement of blocks in cache memory; LRU strategy is often used to decide on which page to replace.

• When the content of a page, which is loaded into main memory, has been modified as result of a write, it has to be written back on the disk after its replacement.

One of the control bits in the page table is used in order to signal that the page has been modified.

Summary

- A memory system has to fit very large programs and still to provide fast access.
- A hierarchical memory system can provide needed performance, based on the locality of reference.
- Cache memory is an essential component of the memory system; it can be a single cache or organized as separate data and instruction caches.
- Cache memories can be organized with Direct Mapping, Set Associative Mapping, and Associative Mapping
- When a new block is brought into the cache, another one has to be replaced; in order to decide on which one to replace different strategies can be used: Random, LRU, FIFO, LFU, etc.
- In order to keep the content of the cache coherent with main memory, certain write strategies have to be used: write-through, write-through with buffered write, copy-back.
- The address space seen by programs is a virtual one and is much larger than the available physical space.
- Demand paging is based on the idea that **only a part of the pages** is in main memory at a certain moment; the OS loads pages into memory when needed.
- The MMU translates a virtual address into a physical one; this is solved using the page table.
- The page table itself is distributed along the memory hierarchy: TLB (cache), main memory, disk.

13.11 CONTROL MEMORY& MICRO-PROGRAM SEQUENCER

We know that there are mainly two different types of control units:

- Microprogrammed and
- Hardwired.

In microprogrammed control, the control signals associated with operations are stored in special memory units inaccessible by the programmer as control words. A control word is a microinstruction that specifies one or more microoperations.

A sequence of microinstructions is called a microprogram, which is stored in a ROM or RAM called a **Control Memory (CM)**. The idea of microprogrammed control is to store the control signals associated with the implementation of a certain instruction as a microprogram in a special memory called a **Control Memory (CM)**.

Microinstructions are fetched from CM the same way program instructions are fetched from main memory.



Fig. 13.11: Fetching Micro-instruction (Control Word)

A microprogram sequencer for generating in a proper sequence the addresses of the successive microinstructions used in executing a given machine instruction includes a PROM next address generator that produces the successive addresses.

The successive addresses are utilized as the successive microinstructions. Each address produced includes a normal next address, but this normal next address may be alterable by address alteration signals that are generated in response to a number of sensed conditions within the computer and in response to predetermined machine instruction register bits. The address alteration of a normal next address, if required, is accomplished within the same clock period in which the normal next address is initially formed, permitting jump or branch instructions to be performed as rapidly as normal instructions.

No mapping PROM, microsequencer counter, no microsequencer incrementer are needed to implement the present invention. A microprogram sequencer for generating in a proper sequence, including required branching, the addresses of the successive microinstructions used in executing a given machine instruction by a computer of the type in which status signals are produced which represent the status of various components of the computer, and in which the operation of the various components is synchronized by a clock which generates a periodic clock signal demarking successively occurring machine cycle clock periods, said **microprogram sequencer** comprising in combination:

Address Generator Memory means for producing during a current machine cycle period a first set of output signals including a first code set of signals designating a normal next input address for said address generator memory means;

Selector means receiving as inputs applied status signals, instruction signals, and predetermined ones of the set of output signals produced by said address generator memory means, and responsive to the received signals during the current machine cycle period for selectively producing address alteration signals during the current machine cycle period;

means for logically combining said address alteration signals and said first code set of signals designating a normal next address during the current machine cycle period to selectively alter the first code set of signals to represent an altered next input address, any alteration of the first code set of signals being established before the end of the current machine cycle period; and means for applying the

first code set of signals to said address generator memory means during the current machine cycle period as the input address thereto, said address generator memory means being responsive to such application of the first code set of signals, whether altered or unaltered, for producing during the next successive machine cycle period a selectively corresponding second set of output signals including a second code set of signals designating the next successive normal input address for said address generator memory means.



Microprogram Sequencer Block Diagram

Fig. 13.12: Block Diagram of Micro-Control Sequencer

13.11.1 Why Control Memory

Control memory is a Random Access Memory (RAM) consisting of addressable storage registers. It is primarily used in mini and mainframe computers. It is used as a temporary storage for data. Access

to control memory data **requires less time than to main memory;** this speeds up CPU operation by reducing the number of memory references for data storage and retrieval. Access is performed as part of a control section sequence while the master clock oscillator is running.

13.12 DEFINING A MICROINSTRUCTION FORMAT

We can choose the number of fields a microinstruction should have and which control signals should be affected by each field. In choosing the format:

(a) simplify the representation

- Ex: The mnemonics Add, Subt and Func can represent the function to be performed by ALU.
- (b) try to make it easier to write and understand microprogram.
- Ex: It is useful to have one field controlling the ALU, two fields to determine the two sources for the ALU, and one field to determine the destination of ALU result

(c) make it difficult to write inconsistent microinstructions.

Ex: From the three write signals *RegWrite*, *MemWrite* and *IRWrite* only one must be asserted in a given cycle. If the mnemonics of these three signals share the same microinstruction field, we can place only one mnemonics to that field, restricting these three signals to one at a time.

In selecting the microinstruction format for MIPS subset multi clock cycle implementation, we can assume that signals that are never asserted simultaneously may share the same field.

We can thus define the following 8 fields:

ALU Control	SRC1	SRC2	ALU Dest.	Memory	Mem. Reg.	PCWrite Control	Sequencing
----------------	------	------	--------------	--------	--------------	--------------------	------------

Fig. 13.13: Instruction Format for MIPS

Field names and their functions:

- 1. ALU Control: Specify the operation to be performed by ALU.
- 2. SRC1: Specify the source for the 1st ALU operand.
- 3. SRC2: Specify the source for 2nd ALU operand.
- 4. ALU Dest.: Specify the register to be written from ALU result.
- 5. Memory: Specify read/write and the address source for memory.
- 6. Memory Reg.: Specify the reg. Destination (for a memory read) or the source of value to be written (for a memory write).
- 7. PCWrite Contr.: Specify the update of PC.
- 8. Sequencing: Specify how to choose the next microinstruction to be executed.

13.13 WHAT IS MICRO-OPERATION

Micro operations: operations executed on data stored in one or more registers. The sequence of micro operations to be performed stored in binary form in the registers. The result of the operation may be:

- · Replace the previous Binary Information of a Register or
- Transferred to another Register

13.14 WHAT IS ADDREES SEQUENCING?

It is the procedure for ensuring that received address messages concerning a call attempt are processed in the correct order. In serial data devices, such as EEPROM, Flash and Hard Drives where data is exchanged serially; addresses need to be sent with the data for each byte or block of data.

In parallel data devices, such as DRAM, an address is sent with every byte. With address sequencing, if the data is sequential and not scattered (see "defragmentation" for hard drives or the use of the TRIM command for SSDs and Flash), special read/write commands that do not need to resend address data can be used. This can speed up data access and, for DRAM, save on battery life by not needing to send an address each time.

Micro-Instruction are stored in control Memory in form of groups and each group is specifying routine each computer instruction has own routine in the control memory to generate part of instruction .each instruction has own microinstruction in given location of control memory

When the execution of instruction is completed, control must be return to fetch routine, this done by executing un-conditional branch microinstruction to the first address of fetch routine

The address sequencing capabilities are required in the following Four situations:

- · Incrementing of control Address Register
- · Unconditional branch or conditional branch depending on status bit
- · Mapping process from the bits of instruction to the address of control memory
- A facility to routine call and return

13.15 WHAT ARE COMPUTER REGISTERS

Computer registers are binary storage device, that group are of various flip-flops and designated by capital letters (sometimes followed by numerals):

- R1: processor register
- MAR: Memory Address Register (holds an address for a memory unit)
- PC: Program Counter
- IR: Instruction Register
- SR: Status Register
- The individual flip-flops in an n-bit register are numbered in sequence from 0 to n-1 (from the right position toward the left position)



Fig. 13.14: Block Diagram of Register

13.15.1 Register Transfer Language (RTL)

A symbolic notation to describe the micro operation transfers among registers:

Examples

• Information transfer from one register to another is described by a *replacement operator:*

 $R2 \leftarrow R1$

- This statement denotes a transfer of the content of register R1 into register R2)
- The transfer happens in one clock cycle
- The content of the R1 (source) does not change
- The content of the R2 (destination) will be lost and replaced by the new data transferred from R1
- · Conditional transfer occurs only under a control condition
 - Representation of a (conditional) transfer

P: R2 \leftarrow R1

- A binary condition (P equals to 0 or 1) determines when the transfer occurs
- The content of R1 is transferred into R2 only if P is 1

Basic Symbols for Register Transfer						
Symbos	Description	Examples				
Letters and numerals	Denotes a register	Mar, R2				
Parenthesis ()	Denotes a part of a register	R2(0-7), R2(L)				
Arrow ←	Denotes transfer of information	$R2 \leftarrow R2$				
Comma,	Separates two microoperations	$R2 \leftarrow R1, R1 \leftarrow R2$				

Table: 13.0 Represent Basic Symbols of Register Transfers

13.16 GLOSSARY

Memory: is used to store Data and Instructions in Binary Form

Memory Hierarchy: is the arrangement of various categories of memories based on size, cost & Speed

Main Memory: is Semiconductor, fast Memory and located close to CPU

Secondary Memory: Direct Accessed, Cheap, Slow and Located remotely to CPU

Cache memory: is a small, very fast memory that retains copies of recently used information from main memory

Cache hit: An access to an item which is in the cache

Cache miss: An access to an item which is not in the cache

Cache hit-rate: The proportion of all memory accesses that are satisfied by the cache

Cache miss-rate: The proportion of all memory accesses that are not satisfied by the cache

Temporal locality (locality in time): If an item is referenced, it will tend to be referenced again soon.

Spacial locality (locality in space): If an item is referenced, items whose addresses are close by will tend to be referenced soon.

Least Recently Used (LRU): The candidate line is selected which holds the block that has been in the cache the longest without being referenced.

First-in-First-Out (FIFO): The candidate line is selected which holds the block that has been in the cache the longest.

Least frequently used (LFU): The candidate line is selected which holds the block that has got the fewest references.

Virtual Memory: use virtual addresses rather than real addresses to store instructions and data

Address Translation: It is the translation of a virtual address into a physical one

Page Table: is the data structure used by a virtual memory system in a computer operating system to store the mapping between virtual addresses and physical addresses

Control Word: is a microinstruction that specifies one or more microoperations.

Micro-Program: A sequence of microinstructions

Control Memory: storation of the control signals in a special memory called a control memory (CM).

Microprogram Sequencer: for generating in a proper sequence the addresses of the successive microinstructions used in executing a given machine instruction includes a PROM next address generator that produces the successive addresses

Micro Operations: operations executed on data stored in one or more registers

Adress Sequencing: It is the procedure for ensuring that received address messages concerning a call attempt are processed in the correct order.

Computer Registers: are binary storage device

13.17 REVIEW QUESTIONS

Q.1 Discuss the main Problems with the Memory System in detail.

Q.2 What is Cache Memory? How it is differ from Main Memory?

Q.3 Discuss the-Cache hit, miss, hit-rate & miss-rate.

Q.4 Write the various cache mapping algorithms.

Q.5 Comapre advantages and dis-advantages of various cache mapping algorithms.

Q.6 What do you understand with Micro-program sequencer Explain with Block Diagram?

Write Short Note On:

- (i) Page Replacement in cache
- (ii) Advantages and Dis-advantages of Direct Mapping
- (iii) Page Replacement-LRU,FFIFO,LFU

- (iv) Virtual Memory
- (v) Page-Table
- (vi) Address Translation
- (vii) Control Word
- (viii) Control Memory
- (ix) Instruction Format
- (x) Micro-Program
- (xi) Micro-operations
- (xii) Address Sequencing
- (xiii) Computer Register
- (xiv) RTL

Differentiate Between Following:

- (i) Main Memory Vs Secondary Memory
- (ii) Cache hit and miss
- (iii) Cache hit-rate & miss-rate
- (iv) Temporal and Spacial Locality
- (v) Write through and write through buffer write
- (vi) Write through and Copy Back
- (vii) Micro-operation and Micro-Program
- (viii) Micro-Instruction and Micro-Operation

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